Introduction to Xilinx Zynq-7000™ All Programmable SoC
Agenda

- **Embedded Processor Challenge**
  - Zynq-7000 AP SoC Family Overview
  - Zynq-7000 AP SoC Ecosystem
  - Zynq-7000 AP SoC HW & SW Design Tools and Flow
  - Zynq-7000 AP SoC Development Kits, Training, and Docs
Embedded Processor Challenge

Which Technology Should I Choose?
# Zynq-7000 AP SoC Value Proposition

Conflicting Demands Now Served by the Xilinx Zynq-7000

<table>
<thead>
<tr>
<th></th>
<th>ASIC</th>
<th>ASSP</th>
<th>2 Chip Solution</th>
<th>Zynq-7000</th>
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<tbody>
<tr>
<td>Performance</td>
<td>+</td>
<td>+</td>
<td>-</td>
<td>+</td>
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<tr>
<td>Power</td>
<td>+</td>
<td>+</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Unit Cost</td>
<td>+</td>
<td>+</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>TCO</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Risk</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>TTM</td>
<td>-</td>
<td>+</td>
<td>+</td>
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<tr>
<td>Flexibility</td>
<td>-</td>
<td>-</td>
<td>+</td>
<td>+</td>
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<tr>
<td>Scalability</td>
<td>-</td>
<td>-</td>
<td>+</td>
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+ positive, - negative, ■ neutral
Course Objectives

- Embedded Processor Challenge
- Zynq-7000 AP SoC Family Overview
- Zynq-7000 AP SoC Ecosystem
- Zynq-7000 AP SoC HW & SW Design Tools and Flow
- Zynq-7000 AP SoC Development Kits, Training, and Docs
Introducing Xilinx Zynq™-7000 AP SoC

- **Complete ARM®-based Processing System**
  - Dual ARM Cortex™-A9 MPCore™, processor centric
  - Integrated memory controllers & peripherals
  - Fully autonomous to the Programmable Logic

- **Tightly Integrated Programmable Logic**
  - Used to extend Processing System
  - Scalable density and performance
  - Over 3000 internal interconnects

- **Flexible Array of I/O**
  - Wide range of external multi-standard I/O
  - High performance integrated serial transceivers
  - Analog-to-Digital Converter inputs
Zynq-7000 can meet customer’s expectations

Programmable Systems Integration

Increased System Performance  BOM Cost Reduction  Total Power Reduction

Accelerated Design Productivity
Zynq-7000: Break-out in Customer Value

● **All Programmable + Systems Integration**
  ○ ARM Cortex™-A9 MPCore™ Processing System with hardened peripherals, ADC and 28nm scalable optimized programmable logic

● **Increased System Performance**
  ○ Dual Core ARM Cortex A9’s with NEON and FPU
  ○ Programmable logic with massive DSP processing
  ○ Optimized & Simplified HW/SW Partitioning, HW Accelerator

● **BOM Cost Reduction**
  ○ Reduced Devices per Board (Processors, PLDs, DSPs, ADC, Power supplies, fans, etc…)
  ○ Reduced PCB Complexity (Fewer traces/interconnect/layers, Fewer power supplies, Smaller overall PCB … )

● **Total Power Reduction**
  ○ Flexible/Tunable Power Envelope
  ○ Integration Power Reduction

● **Accelerated Design Productivity**
  ○ Reduced Time To Market (Ecosystem, HLS, Platform, Plug&Play AXI IP …)
Zynq-7000 AP SoC Block Diagram

Processing System

- Static Memory Controller
  - Quad-SPI, NAND, NOR
- Dynamic Memory Controller
  - DDR3, DDR2, LPDDR2
- AMBA® Switches
  - ARM® CoreSight™ Multi-core & Trace Debug
  - NEON™/FPU Engine
  - Cortex™-A9 MPCore™ 32/32 KB I/D Caches
  - Timer Counters
  - General Interrupt Controller
  - Snoop Control Unit (SCU)

I/O MUX

- 2x SPI
- 2x I2C
- 2x CAN
- 2x UART
- GPIO
- 2x SDIO with DMA
- 2x USB with DMA
- 2x GigE with DMA

EMIO

XADC

M_AXI_GP0/1

S_AXI_GP0/1

M_AXI_ACP

Programmable Logic:

- System Gates, DSP, RAM

S_AXI_HP0

S_AXI_HP1

S_AXI_HP2

S_AXI_HP3

S_AXI_ACP

Multi-Standards I/Os (3.3V & High Speed 1.8V)

PCIe

Multi Gigabit Transceivers

Multi-Standards I/Os (3.3V & High Speed 1.8V)
Real Zynq-7000 AP SoC Silicon (XC7Z020)
ARM Cortex-A9 Processor and L1 Caches

- **ARM Cortex-A9 processor key features**
  - 2.5 DMIPS/MHz or 11.5 CoreMark™/MHz per core
  - Up to 800MHz/1GHz operation
  - Harvard architecture, 64-bit data and 64-bit instruction interfaces
  - Little endian support for both instruction and data

- **ARM Cortex-A9 processor L1 cache key features**
  - 32KB Instruction and 32KB Data cache
  - The cache line length is eight words (32 bytes)
  - 4-way set associative, write-back
  - All L1 caches support parity

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>ARM® CoreSight™ Multi-core &amp; Trace Debug</td>
<td>NEON™/FPU Engine</td>
</tr>
<tr>
<td>NEON™/FPU Engine</td>
<td>NEON™/FPU Engine</td>
</tr>
<tr>
<td>Cortex™-A9 MPCore™ 32/32 KB I/D Caches</td>
<td>Cortex™-A9 MPCore™ 32/32 KB I/D Caches</td>
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<tr>
<td>Snoop Control Unit (SCU)</td>
<td>Timer Counters</td>
</tr>
<tr>
<td>256 KB On-Chip Memory</td>
<td>General Interrupt Controller</td>
</tr>
<tr>
<td>DMA</td>
<td>Configuration</td>
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</tbody>
</table>
NEON

- NEON technology is wide Single Instruction Multiple Data (SIMD) parallel & co-processing architecture
  - Extension of ARM instruction set – not a standalone DSP processor

- Applications
  - For real-time soft codec performance, able to keep up with evolving Codec standards
  - Video encode/decode
  - 2D/3D graphics,
  - Audio and speech processing,
  - Image processing

- Fewer cycles needed as compared to ARM CPU only
  - Rule of thumb: NEON optimizations will half number of cycles for entire codec
FPU

- High performance single/double precision VFPv3 FPU
  - Includes half-precision conversions (FP16) useful for graphics & audio

- Register set shared with NEON
  - Requires crafting of NEON and FPU code versus pure FPU code for hand crafted code
  - Expands the size of the FPU register set

- Compliant with IEEE-754 standard (with noted exceptions)

- Floating Point Performance is:

<table>
<thead>
<tr>
<th>CPU MHz</th>
<th>MFLOPs/MHz*</th>
<th>1 CPU GFLOPs</th>
<th>2 CPU GFLOPs</th>
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<tbody>
<tr>
<td>800</td>
<td>2</td>
<td>1.6</td>
<td>3.2</td>
</tr>
<tr>
<td>667</td>
<td>2</td>
<td>1.3</td>
<td>2.7</td>
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<tr>
<td>533</td>
<td>2</td>
<td>1.1</td>
<td>2.1</td>
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<tr>
<td>400</td>
<td>2</td>
<td>0.8</td>
<td>1.6</td>
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</tbody>
</table>
SCU and ACP

**Snoop Control Unit (SCU) Features**
- L1 Cache Snoop Control
  - Coherent option for multi-core software development
  - Snoop filtering monitors cache traffic
  - High performance cache-to-cache transfers
  - Accelerator Coherency Port

**Accelerator Coherence Port**
- Accelerators gain access to CPU cache hierarchy
- Uses AMBA® 3 AXI™ technology for compatibility with standard un-cached
- Supported in hardware - no software needed
- Allows coherency to be extended to PL
The rest of APU

- **General Interrupt Controller**
  - Ability to route interrupts to either CPU or both CPUs
  - Supports 53 interrupts (16 dedicated to the Programmable Logic)

- **On Chip Memories (OCM)**
  - Boot ROM (not user accessible)
  - 256 KB shared SRAM with parity

- **Central DMA (8 Channels)**
  - 4 for the Processing System
  - 4 for the Programmable Logic
  - Dedicated synchronization signals to PL

- **Device Configuration (DEVC)**
  - Interface to configure Programmable Logic

- **Private Watch Dog Timer and Timer for each CPU**
- **System Watch Dog and Triple Timer Counters**
- **ARM CoreSight Debug Technology**
Hardware/Software Debug Support

- **One-cable solution (cascaded JTAG)**
  - Xilinx cable connected to the Xilinx JTAG
    - ARM Debug Access Port (DAP) in front of Xilinx JTAG in the chain
    - Software debug with SDK
    - Hardware debug with ChipScope
    - iMPACT bitstream download

- **Two-cable solution (independent JTAG)**
  - Xilinx cable connected to the Xilinx JTAG
    - Hardware debug with ChipScope
    - iMPACT bitstream download
  - ARM DSTREAM/3rd party cable connected to DAP
    - Software debug using ARM/3rd party tools

- **CoreSight™ (Processor Trace)**
  - 16-bit via MIO, 125MHz internal clock, sampled at both edges of the clock
  - 32-bit via EMIO, 250MHz EMIOTRACECLK, sampled at the rising clock edge
Memory Controller in Zynq-7000

- **DDR controller**
  - DDR3, DDR2, and LPDDR2
  - 16 bit or 32 bit wide; ECC on 16 bit
  - DDR3 @ 1.5V up to DDR1333
  - DDR2 @ 1.8V up to DDR800
  - LPDDR2 @ 1.2V up to DDR800
  - 73 dedicated DDR pins
  - Credit-based round robin arbitration
  - No DIMM support

- **NAND Controller**
  - ECC
  - 8 bit or 16 bit data widths

- **NOR/SRAM Controller**
  - 8 bit data width

- **Quad SPI (QSPI) Controller**
  - Up to 2 QSPI parallel memories
PS Common Peripherals

- Two USB 2.0 OTG/Device/Host
  - ULPI, 12 Endpoints
  - Full and High Speed support

- Two Tri-Mode GigE (10/100/1000)
  - IEEE1588 rev 2.0

- Two SD/SDIO interfaces
  - Memory, IO and combo cards

- Two CAN 2.0B, SPI, I2C, UART

- Four GPIO 32bit Blocks

- Multiplexed Input/Output (MIO)
  - Multiplexed output of peripheral and static memories
  - Two I/O Banks: each selectable - 1.8V, 2.5V or 3.3V
  - Configured using new feature in XPS

- Extended MIO
  - Enables use of Select IO with PS peripherals
Zynq-7000 Configuration and Boot

- **Processor First! CPU configures the PS and PL**
  - Standalone PL configuration (without PS configuration) is not supported
  - Configuration under external host control is also possible via JTAG

- **Two boot modes**
  - Secure boot
  - Non-secure boot

- **Four master boot methods (secure or non-secure boot)**
  - QSPI (16MB, 50MB/Sec)*
  - NOR (64MB, 20MB/Sec)
  - NAND (tested up to 1GB, 10MB/Sec)*
    - * cannot be used in the same design
  - SD (Up to 32GB)

- **One slave boot method (non-secure)**
  - JTAG for debug and development
Booting Linux on Zynq-7000

- Example of Zynq-7000 booting Linux
  - BOOT.BIN on SD Card
# Zynq-7000 AP SoC Product Table

<table>
<thead>
<tr>
<th>Devices Name</th>
<th>Z-7010</th>
<th>Z-7015</th>
<th>Z-7020</th>
<th>Z-7030</th>
<th>Z-7045</th>
<th>Z-7100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Number</td>
<td>XC7Z010</td>
<td>XC7Z015</td>
<td>XC7Z020</td>
<td>XC7Z030</td>
<td>XC7Z045</td>
<td>XC7Z100</td>
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## Processing System

<table>
<thead>
<tr>
<th></th>
<th>Z-7010</th>
<th>Z-7015</th>
<th>Z-7020</th>
<th>Z-7030</th>
<th>Z-7045</th>
<th>Z-7100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Core</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Processor Extensions</td>
<td></td>
<td>NEON™ &amp; Single / Double Precision Floating Point</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max Frequency</td>
<td>800MHz</td>
<td></td>
<td></td>
<td></td>
<td>1GHz</td>
<td></td>
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<tr>
<td>Memory</td>
<td>L1 Cache 32KB I / D, L2 Cache 512KB, on-chip Memory 256KB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>External Memory Support</td>
<td>DDR2, DDR3, LPDDR2, 2x QSPI, NAND, NOR</td>
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<td></td>
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<tr>
<td>Peripherals</td>
<td>2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 32b GPIO</td>
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<td></td>
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## Programmable Logic

<table>
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<tr>
<th>Logic Architecture</th>
<th>Artix-7 FPGA</th>
<th>Kintex-7 FPGA</th>
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<td>6-input Look-Up Table (LUT)</td>
<td>17,600</td>
<td>46,200</td>
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<tr>
<td>Flip-Flops</td>
<td>35,200</td>
<td>92,400</td>
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<tr>
<td>Extensible Block RAM (# of Blocks)</td>
<td>240KB (60)</td>
<td>340KB (95)</td>
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<tr>
<td>Peak DSP Performance (Symmetric FIR)</td>
<td>100 GMACs</td>
<td>100 GMACs</td>
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<tr>
<td>PCI Express® (Root Complex or Endpoint)</td>
<td>Gen2 x 4</td>
<td>Gen2 x4</td>
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<tr>
<td>Analog to Digital Converters (ADC)</td>
<td>Dual 12bit 1Msp A/D Converter</td>
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</table>

## IO

<table>
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<th>Z-7030</th>
<th>Z-7045</th>
<th>Z-7100</th>
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<td>Multi Standards 3.3V IO</td>
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<td>Multi Standards High Performance 1.8V IO</td>
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<td>Multi Gigabit Transceivers</td>
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## Zynq-7000 AP SoC Package Table

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<th>Z-7015</th>
<th>Z-7020</th>
<th>Z-7030</th>
<th>Z-7045</th>
<th>Z-7100</th>
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<tbody>
<tr>
<td>Part Number</td>
<td>XC7Z010</td>
<td>XC7Z015</td>
<td>XC7Z020</td>
<td>XC7Z030</td>
<td>XC7Z045</td>
<td>XC7Z100</td>
</tr>
<tr>
<td>Package Type</td>
<td>CLG225</td>
<td>CLG400</td>
<td>CLG485</td>
<td>CLG400</td>
<td>FBG484</td>
<td>FBG676</td>
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<tr>
<td>Package Size (mm)</td>
<td>13 x 13</td>
<td>17 x 17</td>
<td>19 x 19</td>
<td>17 x 17</td>
<td>23 x 23</td>
<td>27 x 27</td>
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<tr>
<td>Pitch (mm)</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>1.0</td>
<td>1.0</td>
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<td>PS MIOs</td>
<td>32</td>
<td>54</td>
<td>54</td>
<td>54</td>
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<td>54</td>
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<td>HR IO (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)</td>
<td>54 100 150 125 200 100</td>
<td>100 100 100 100 100 212</td>
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<td>HP IO (1.2V, 1.35V, 1.5V, 1.8V)</td>
<td>- - - 63 150 150</td>
<td>150 150 150 150 150 150</td>
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<tr>
<td>Serial Transceiver</td>
<td>- - 4 - 4 8 16</td>
<td>16 16 16</td>
<td></td>
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<tr>
<td>Max Transceiver Speed</td>
<td>N/A N/A 5.4 Gbps</td>
<td>N/A N/A 6.6 Gbps 6.6 Gbps 12.5 Gbps 6.6 Gbps 12.5 Gbps 10.3 Gbps 10.3 Gbps</td>
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22
# Zynq-7000 AP SoC Temperature Range

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<tr>
<th>Grade</th>
<th>-1C</th>
<th>-1I</th>
<th>-2I</th>
<th>-2E</th>
<th>-3E</th>
<th>-1Q</th>
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<td>Z-7010</td>
<td>yes</td>
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<td>yes</td>
<td>yes</td>
<td>yes</td>
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<td>Z-7015</td>
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<td>no</td>
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<tr>
<td>Z-7020</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
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<tr>
<td>Z-7030</td>
<td>yes</td>
<td>yes</td>
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<td>yes</td>
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<td>Z-7045</td>
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<td>Z-7100</td>
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<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>N.A</td>
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</tbody>
</table>

- **C Grade**: 0°C to +85°C
- **E Grade**: 0°C to +100°C
- **I Grade**: -40°C to +100°C
- **Q Grade**: -40°C to +125°C
Course Objectives

- Embedded Processor Challenge
- Zynq-7000 AP SoC Family Overview
- **Zynq-7000 AP SoC Ecosystem**
- Zynq-7000 AP SoC HW & SW Design Tools and Flow
- Zynq-7000 AP SoC Development Kits, Training, and Docs
Zynq-7000 Extensive Partnership Ecosystem

And MORE …
# Operating Systems Support & Status

<table>
<thead>
<tr>
<th>OS</th>
<th>Provider</th>
<th>Version</th>
<th>Availability (ZC702 board support)</th>
<th>Segment Market</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux</td>
<td>ENEA</td>
<td>3.0</td>
<td>Now</td>
<td>Used in all segments</td>
</tr>
<tr>
<td>ENEA Linux</td>
<td>ENEA</td>
<td>3.0</td>
<td>Now</td>
<td></td>
</tr>
<tr>
<td>WR Linux 5</td>
<td>Wind River</td>
<td>3.4</td>
<td>Now</td>
<td></td>
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<tr>
<td>MVL CGE6</td>
<td>Montavista</td>
<td>2.6.32</td>
<td>Jan ‘13</td>
<td>Communications</td>
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<tr>
<td>LinuxLink</td>
<td>Timesys</td>
<td>NA</td>
<td>Now</td>
<td>Industrial, Medical, Automotive</td>
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<tr>
<td>Android</td>
<td>iVela</td>
<td>2.3</td>
<td>Now</td>
<td>Consumer</td>
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<td>Windows Embedded</td>
<td>Adeneo Embedded</td>
<td>7</td>
<td>Now</td>
<td>ISM, Automotive</td>
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<td>Compact 7</td>
<td>Wind River</td>
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<td>Now</td>
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<td>ISM, Automotive, A&amp;D</td>
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<td>INTEGRITY</td>
<td>GreenHills Software</td>
<td>NA</td>
<td>Now</td>
<td>A&amp;D, Automotive, ISM</td>
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<td>QNX</td>
<td>Adeneo Embedded</td>
<td>6.5</td>
<td>April ‘13</td>
<td>Automotive, ISM</td>
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<td>OSE</td>
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<td>5.5</td>
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<td>Communication</td>
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<td>ThreadX/NetX</td>
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<td>FreeRTOS</td>
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<td>All segments</td>
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<td>RTA-OS SC1-4</td>
<td>ETAS</td>
<td>3.0</td>
<td>Now (single core)</td>
<td>Automotive</td>
</tr>
<tr>
<td>eCOS</td>
<td>ITR</td>
<td>3.0</td>
<td>Q4CY2012</td>
<td>ISM, Automotive</td>
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<tr>
<td>eT-Kernel</td>
<td>eSOL</td>
<td>TBD</td>
<td>Now</td>
<td>Automotive, Consumer</td>
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<td>µc/OS</td>
<td>Micrium</td>
<td>II</td>
<td>Now</td>
<td>Industrial, Medical, A&amp;D</td>
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<td>Nucleus</td>
<td>Mentor</td>
<td>NA</td>
<td>Now</td>
<td>Industrial, Medical and Automotive</td>
</tr>
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<td>Quadros</td>
<td>Quadros</td>
<td>NA</td>
<td>Now</td>
<td>Industrial, Medical, POS</td>
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Course Objectives

- Embedded Processor Challenge
- Zynq-7000 AP SoC Family Overview
- Zynq-7000 AP SoC Ecosystem
- Zynq-7000 AP SoC HW & SW Design Tools and Flow
- Zynq-7000 AP SoC Development Kits, Training, and Docs
Zynq-7000 AP SoC Embedded Design Flow

Vivado™ HLS

Software Developer
- Programming
- Integrate IP
- Test
- Debug

System Architect
- Custom IP
- Partner IP

Hardware Designer
- Design
- Integrate IP
- Test
- Debug

Xilinx™ SDK

ARM DS-5™

Xilinx ISE®

Xilinx XPS

System Generator

Application Processor
- ELF

Programmable Logic
- Bitstream

Zynq-7000 AP SoC

AVNET
electronic marketing
Getting Started: Adding an Embedded Source

1. Create Embedded Source in PlanAhead
2. Customize Zynq Processor in XPS
Configure PS

Configure Clocks

Select UART and assign pin locations

Configure Memory Controller
How is XPS Related to SDK?

PlanAhead/XPS

- Define PS Subsystem
- Configure MIO Peripherals
- Connect PL hardware to PS

Software Development Kit

- Build ARM executable and debug directly on target hardware
- Auto-generate BSP, FSBL targeted to hardware
## Software Development Tools

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<td>Platform Studio SDK (Eclipse IDE) ARM GNU CC</td>
<td>ARM® Development Studio IDE (DS-5)</td>
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<td>RVI Debug DSTREAM Trace</td>
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### JTAG / ARM CoreSight™ Infrastructure
Course Objectives

- Embedded Processor Challenge
- Zynq-7000 AP SoC Family Overview
- Zynq-7000 AP SoC Ecosystem
- Zynq-7000 AP SoC HW & SW Design Tools and Flow
- Zynq-7000 AP SoC Development Kits, Training, and Resources
Zynq-7000 Development Kits

- Learn more about the Zynq-7000 AP SoC
  - Visit www.xilinx.com/zynq

- Purchase a Zynq development kit

ZedBoard
www.zedboard.org
P/N: AES-Z7EV-7Z020-G
Price: $395
Available: July 2012

ZC702 Evaluation Kit
www.xilinx.com/zc702
P/N: EK-Z7-ZC702-CES-G
Price: $895
Available: June 2012

Zynq Video & Imaging Kit
P/N: EK-Z7-VIDEO-CES-G
Price: $1495
Available: June 2012
Where to get more trainings

Xilinx Authorized Training Partner (ATP) Courses

- **Accelerating Design Productivity with SDK**
  - Processors, Peripherals, and Tool Utilization
  - Application Profiling Techniques
  - Writing Custom Device Drivers

  Embedded Systems Software Design
  (2 Days, Level 3)
  [www.xilinx.com/training/atp.htm](http://www.xilinx.com/training/atp.htm)

- **Details of Using Zynq Processor**
  - Advanced Boot Methodologies
  - Cortex-A9 Processor Services
  - Advanced DMA Controller

  Advanced Features and Techniques of Embedded Systems Software Design
  (1 Day, Level 4)
  [www.xilinx.com/training/atp.htm](http://www.xilinx.com/training/atp.htm)

Online Resources

- Xilinx Zynq Linux Wiki
  [wiki.xilinx.com/zynq-linux](http://wiki.xilinx.com/zynq-linux)

- Xilinx Design Tools

- ZedBoard Community (tutorials, forums)
  [www.zedboard.org](http://www.zedboard.org)

- Avnet Online OnDemand Trainings
  [www.zedboard.org](http://www.zedboard.org)
Thank you.