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ALL PROGRAMMABLE™

Automatic Test Equipment Solution

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Agenda

- Automatic Test Equipment Test Object
- Automatic Test Equipment Solution Demand
- Automatic Test Equipment Solution Implementation Method

Automatic Test Equipment Test Object

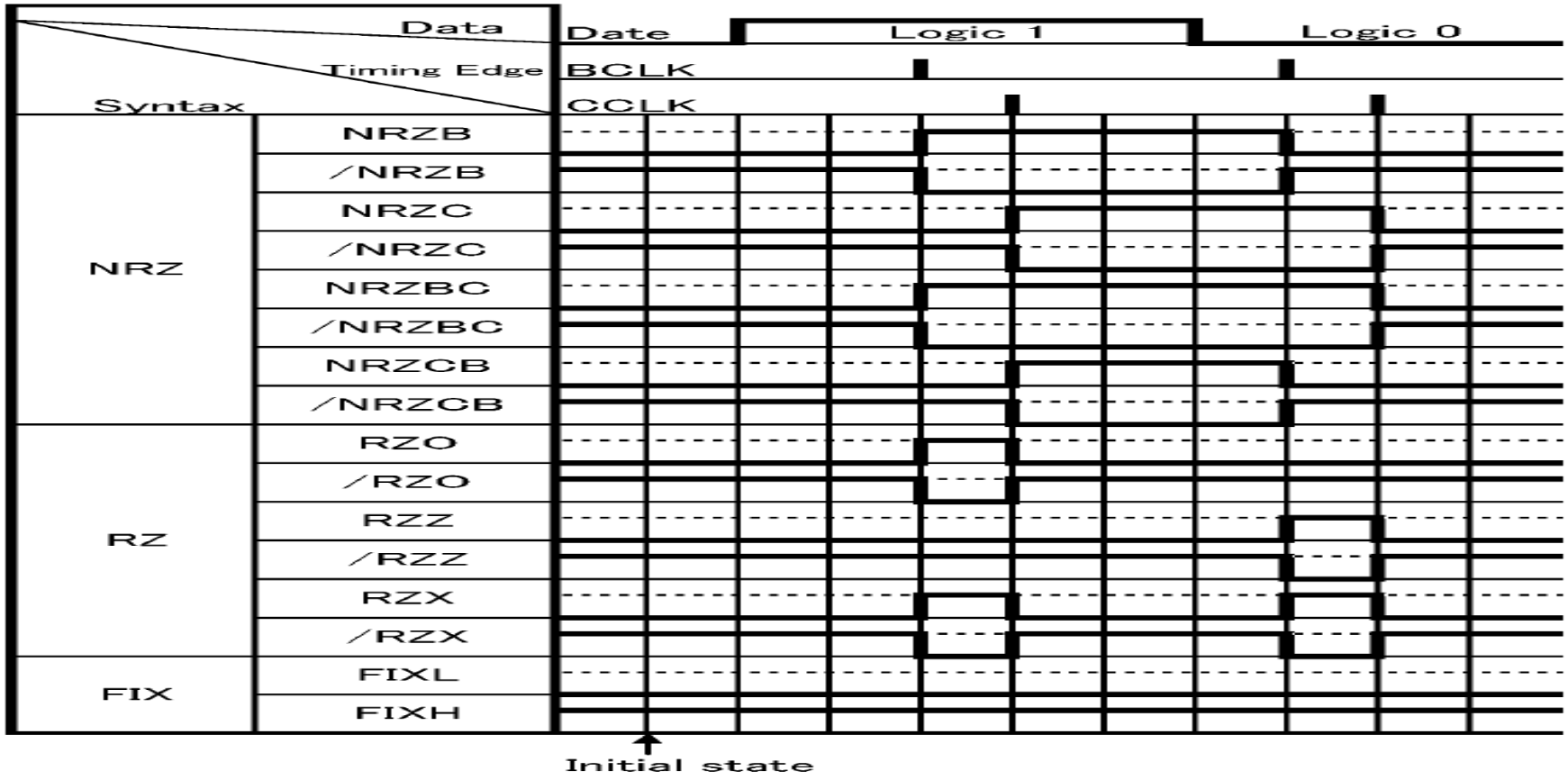
- Automatic Test Equipment Test Object is to Test Tolerance of communication interface .
- Which communication interfaces can be tested?

  E.g. : ONFI 1.0/2.0/2.1/2.2/2.3/3.0 ;CFI / SPI ..
- Different test objects, using different firmware, the hardware is basically similar.

Automatic Test Equipment Solution Demand

Two Demands in this solution

1. One is to the interface timing , Interface timing contains control signal timing and data timing .
2. Control signal timing composition :



Automatic Test Equipment Solution Demand

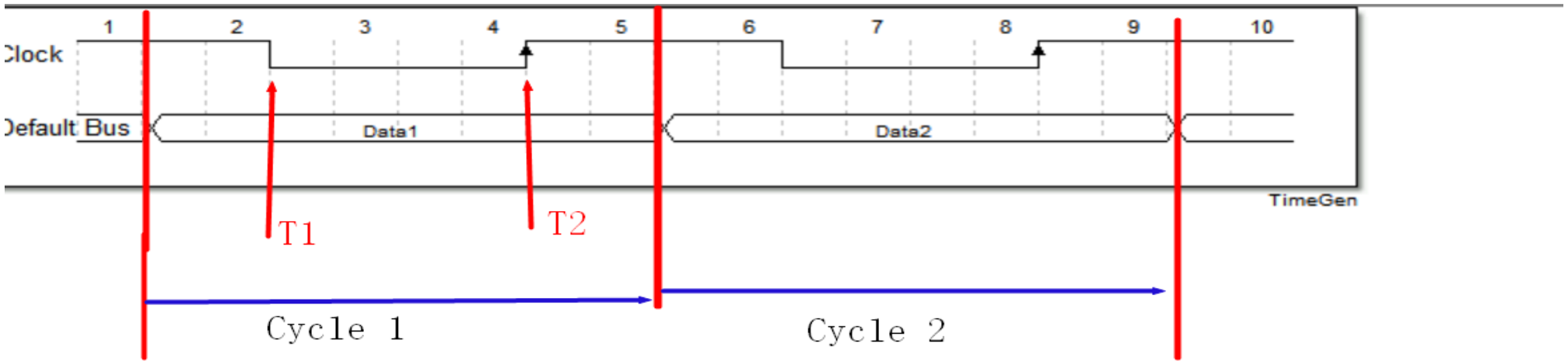
- Control Signal Timing Demand ：

1. Multi-Period cycle output to IO pin. Without delay during cycle transfer. Frequency from 1Mhz to 200Mhz.
2. The cycle generated base on user register with is pre-defined in PLL or read from DDR buffer.
3. Next example is to show 2 types of cycle matching, in real case, it needs select 16 types of cycles to be matching together by user program. (example is T1-T2-T1….., real case is T1,T1,T2,T3,T1,T2,T2,T6,T6,T1…….)

Automatic Test Equipment Solution Demand

Data Timing Demand:

1. After the control signal sequence, it is necessary to control the nanosecond delay to send data
2. Data Timing Demand, After the arrival of the effective signal, the data can be given a fixed delay, the delay level of nanosecond .



Automatic Test Equipment Solution Implementation Method

- Control Signal Timing Demand :In this scheme, the timing of sequential control signal is a difficult problem, and the method of implementation is controlled by 7 Series FPGAs Transceivers wizard concatenation and transformation .

7 Series FPGAs Transceivers Wizard (3.6)

Documentation | IP Location | Switch to Defaults

Component Name: gtwizard_0

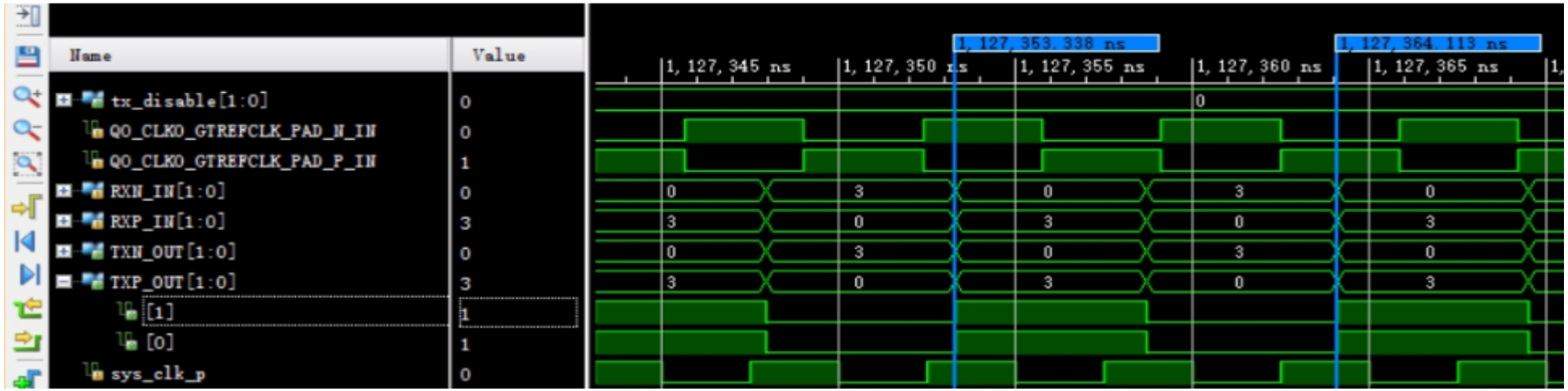
GT Selection | Line Rate, RefClk Selection | Encoding and Clocking | Comma Alignment and Equalization | PCIe, SATA, PRBS | CB and CC Sequence | **Summary**

Summary

Features	GT
Protocol File	Start from scratch
TX Line Rate(Gbps)	2.97
TX reference clock(MHz)	148.500
Encoding	None
TX Internal Data width	16
TX External Data width	32
TXUSRCLK(MHz)	185.625
TXUSRCLK2(MHz)	92.8125
TX Buffer Enabled	true
RX Line Rate(Gbps)	2.97
RX reference clock(MHz)	148.500
Decoding	None
RX Internal Data width	16
RX External Data Width	32
RXUSRCLK(MHz)	185.625
RXUSRCLK2(MHz)	92.8125
RX Buffer Enabled	true

Automatic Test Equipment Solution Implementation Method

- The Simulation waveform and measured waveform.

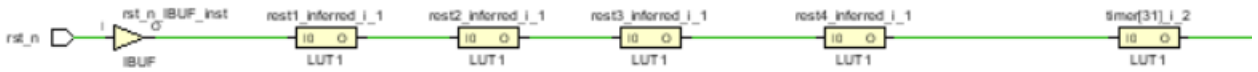


Automatic Test Equipment Solution Implementation Method

- Data Timing Demand Implementation Method .
- Data latency can be achieved using internal logic , To prevent the delay from being optimized, the primitive can be used .
- E.g :

```
(* mark_debug ="ture" *) wire rest1;
(* mark_debug ="ture" *) wire rest2;
(* mark_debug ="ture" *) wire rest3;
(* mark_debug ="ture" *) wire rest4;

not i0 (rest1,rst_n);
not i1 (rest2,rest1);
not i2 (rest3,rest2);
not i3 (rest4,rest3);
```



Thanks