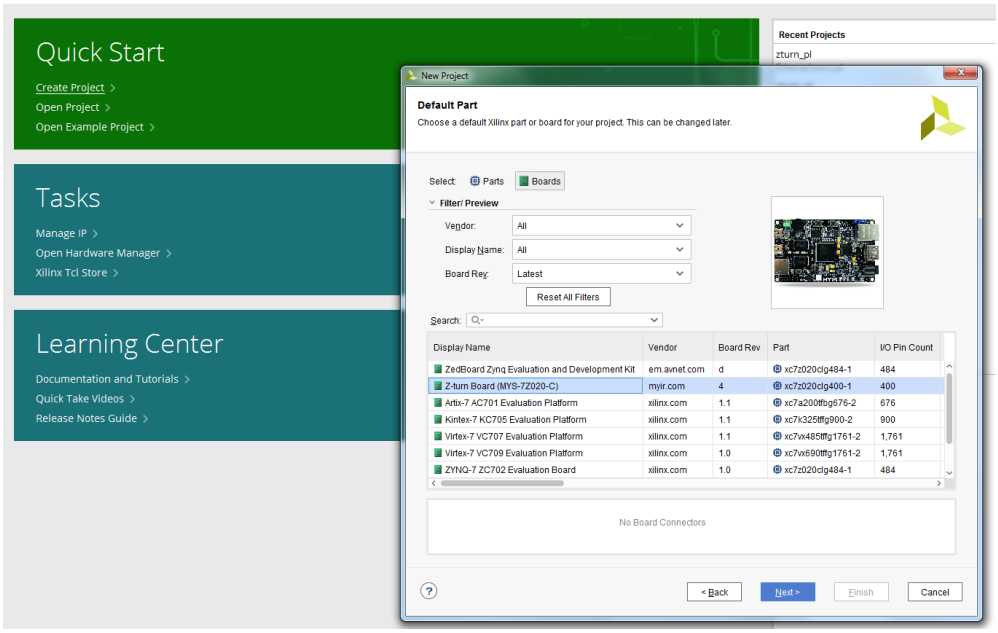
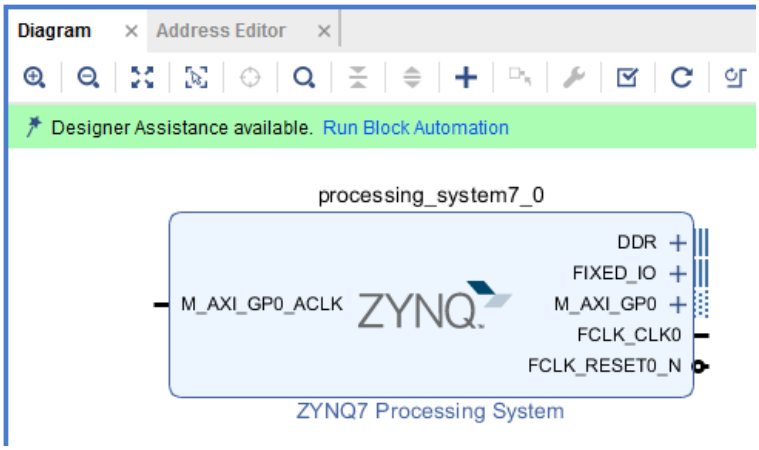
1- Created New Project **ZYNQ_Hello** in VIVADO 2017.3 and select **Z-Turn 7C020 Board**

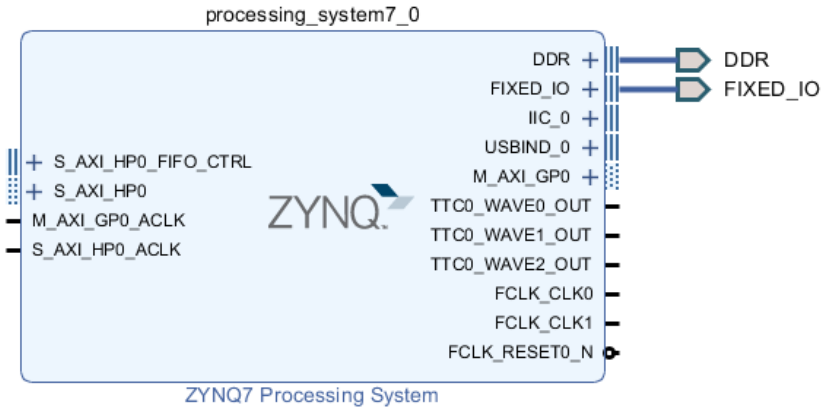


2- Create New Block Diagram

3- Add the **ZYNQ PS** in Block Diagram



4- Click **Run Block Automation**



5- Double click **ZYNQ PS** and disable the followings

QSPI Flash

S_AXI_HP0

FCLK CLK 1

Ethernet

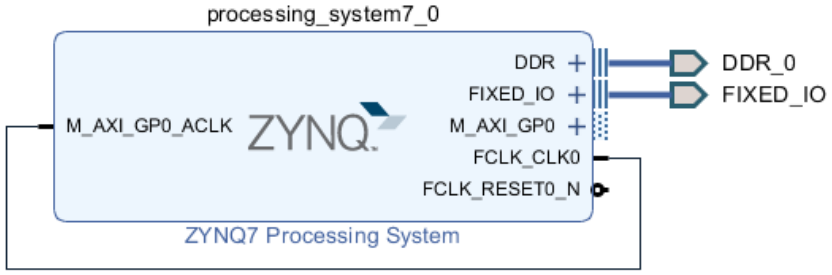
USB

CAN

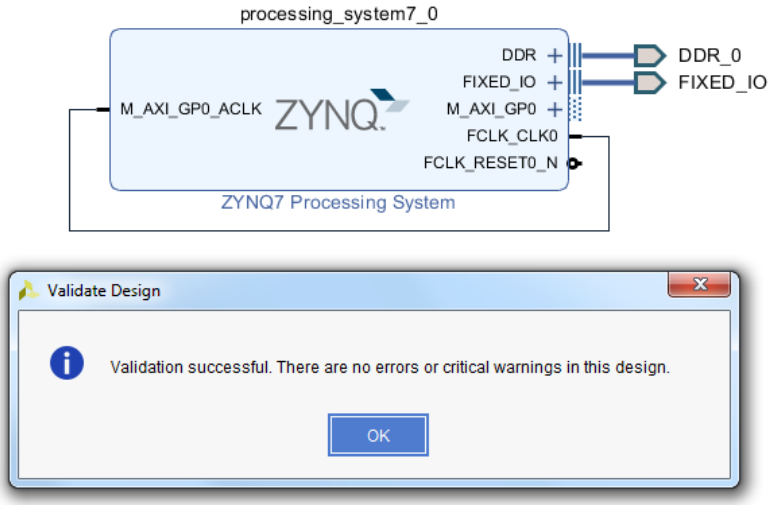
I2C

UART 0

TTC

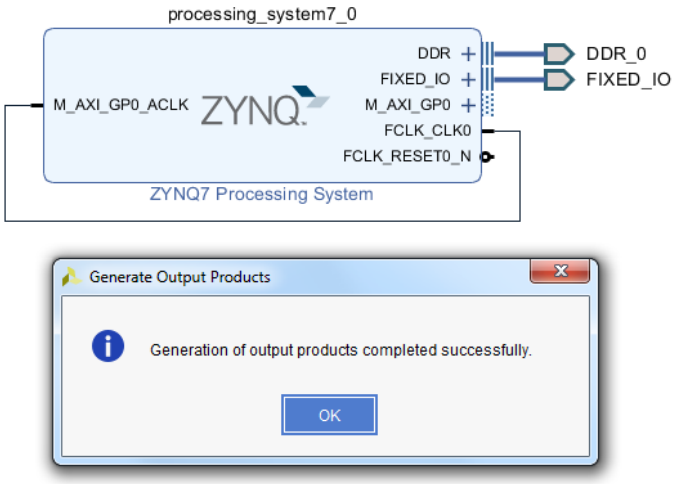


6- Right click **Validate Design**



7- Sources = > Right Click => **Create HDL Wrapper**

8- **Generate Output Product**

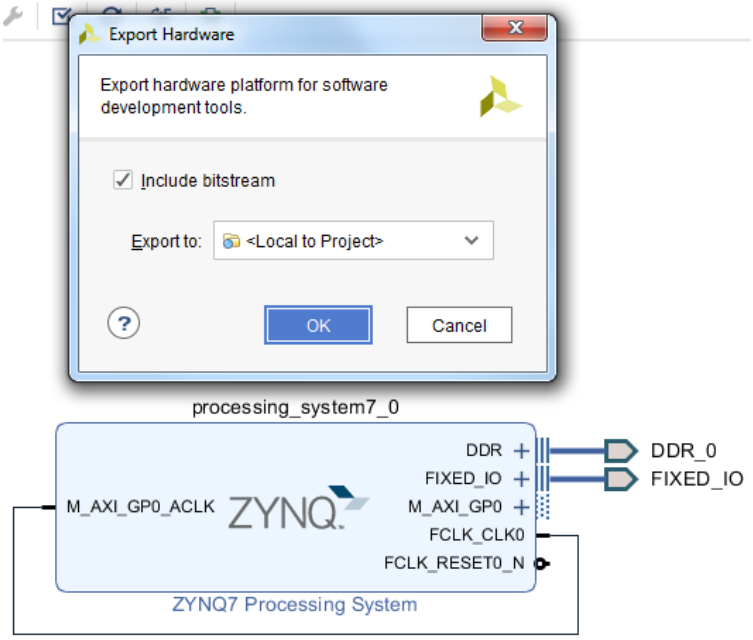


9- **Run Synthesis**

10- **Run Implementation**

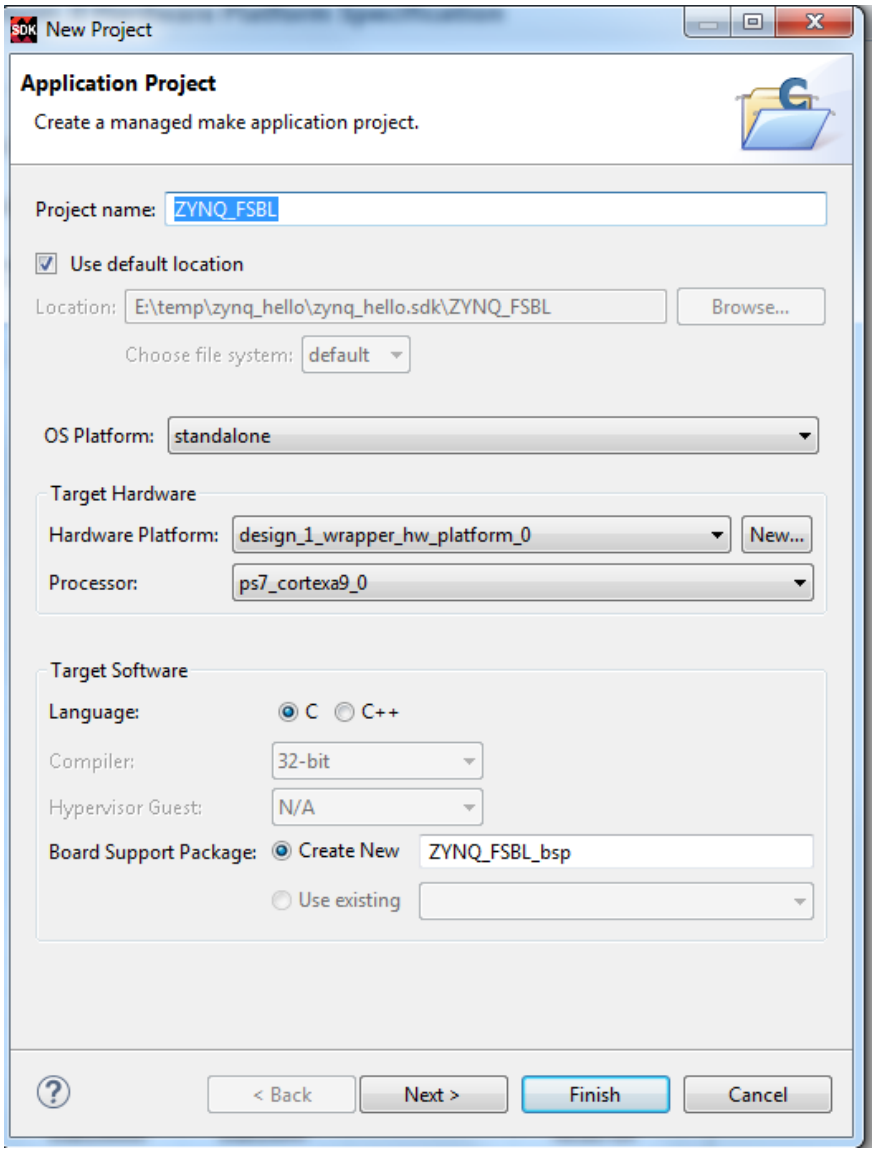
11- **Generate Bitstream**

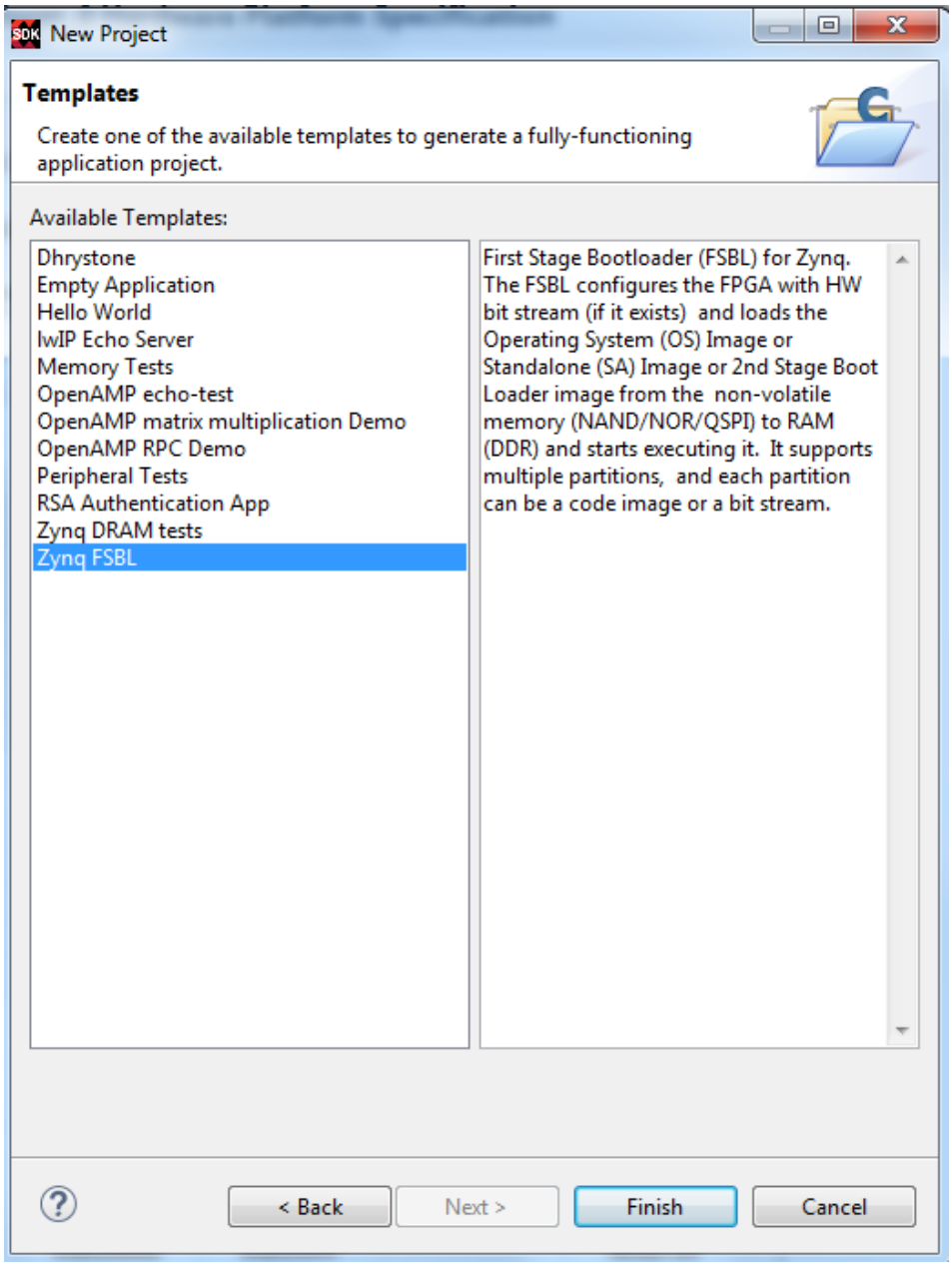
12- File => **Export Hardware include Bitstream**



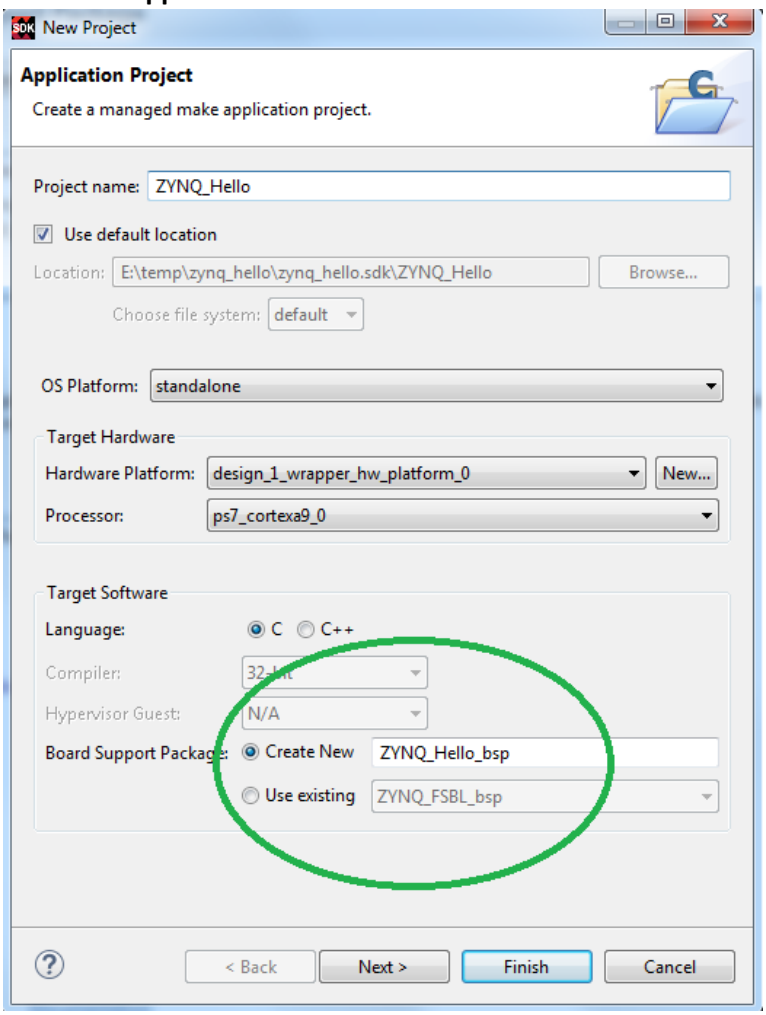
13- File => **Launch SDK**

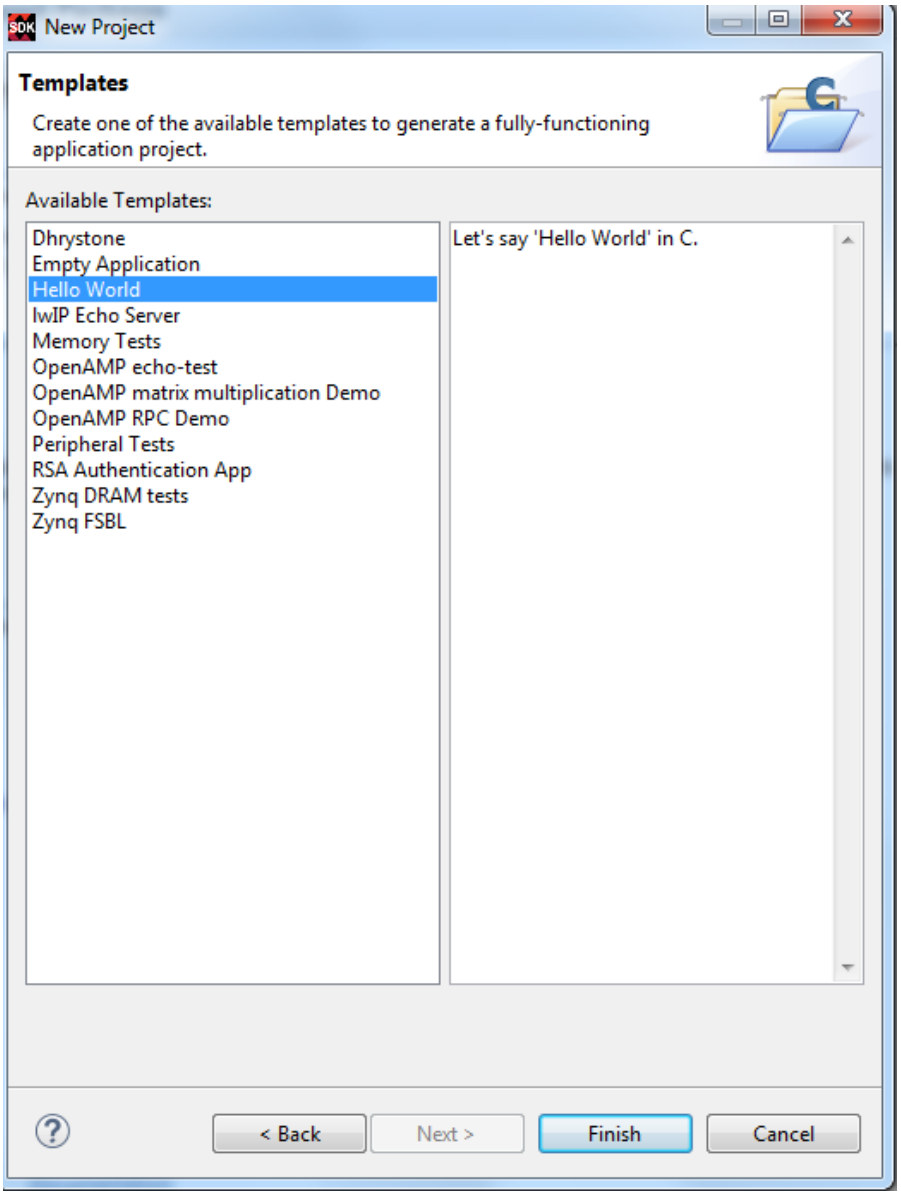
14- Create New **FSBL Application**


New Project
Application Project
Create a managed make application project.
Project name:
ZYNQ_FSBL
Use default location
Location:
E:\temp\zynq_hello\zynq_hello.sdk\ZYNQ_FSBL
Browse...
Choose file system:
default
OS Platform:
standalone
Target Hardware
Hardware Platform:
design_1_wrapper_hw_platform_0
New...
Processor:
ps7_cortexa9_0
Target Software
Language:
C
C++
Compiler:
32-bit
Hypervisor Guest:
N/A
Board Support Package:
Create New
ZYNQ_FSBL_bsp
Use existing
< Back
Next >
Finish
Cancel

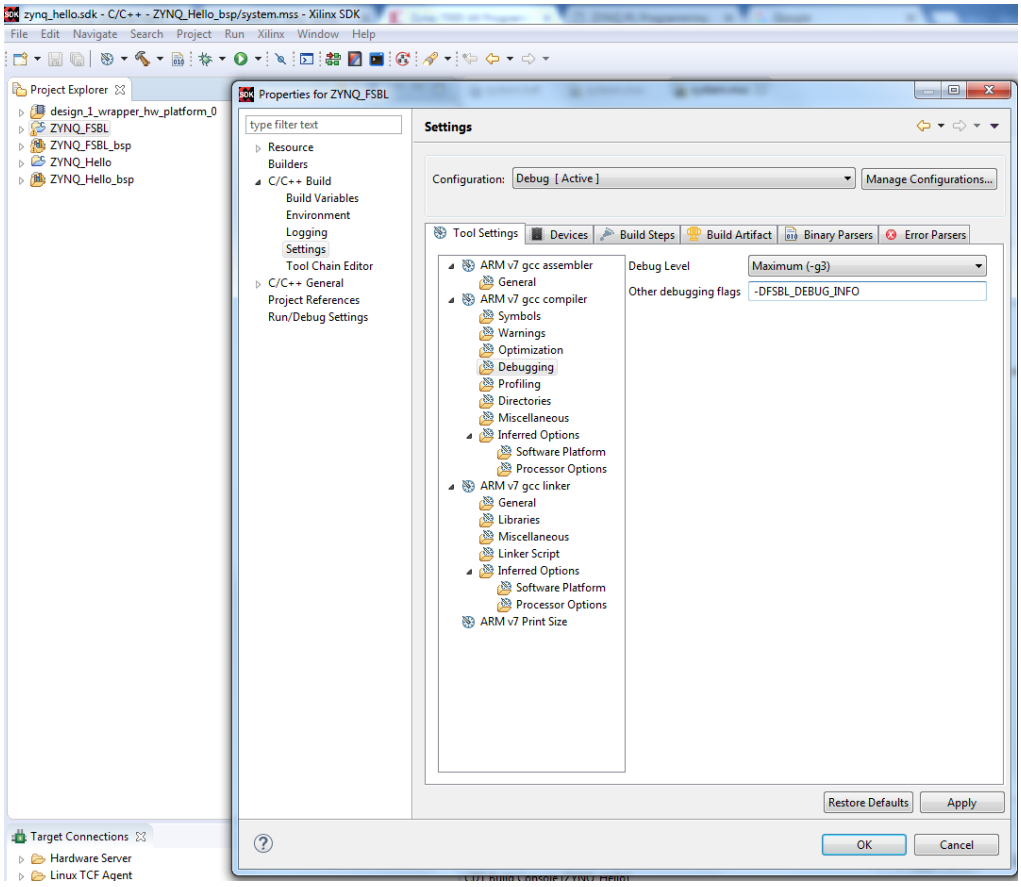

New Project
Templates
Create one of the available templates to generate a fully-functioning application project.
Available Templates:
Dhrystone
Empty Application
Hello World
lwIP Echo Server
Memory Tests
OpenAMP echo-test
OpenAMP matrix multiplication Demo
OpenAMP RPC Demo
Peripheral Tests
RSA Authentication App
Zynq DRAM tests
Zynq FSBL
First Stage Bootloader (FSBL) for Zynq. The FSBL configures the FPGA with HW bit stream (if it exists) and loads the Operating System (OS) Image or Standalone (SA) Image or 2nd Stage Boot Loader image from the non-volatile memory (NAND/NOR/QSPI) to RAM (DDR) and starts executing it. It supports multiple partitions, and each partition can be a code image or a bit stream.
< Back
Next >
Finish
Cancel

15- Create **New Hello World Application**

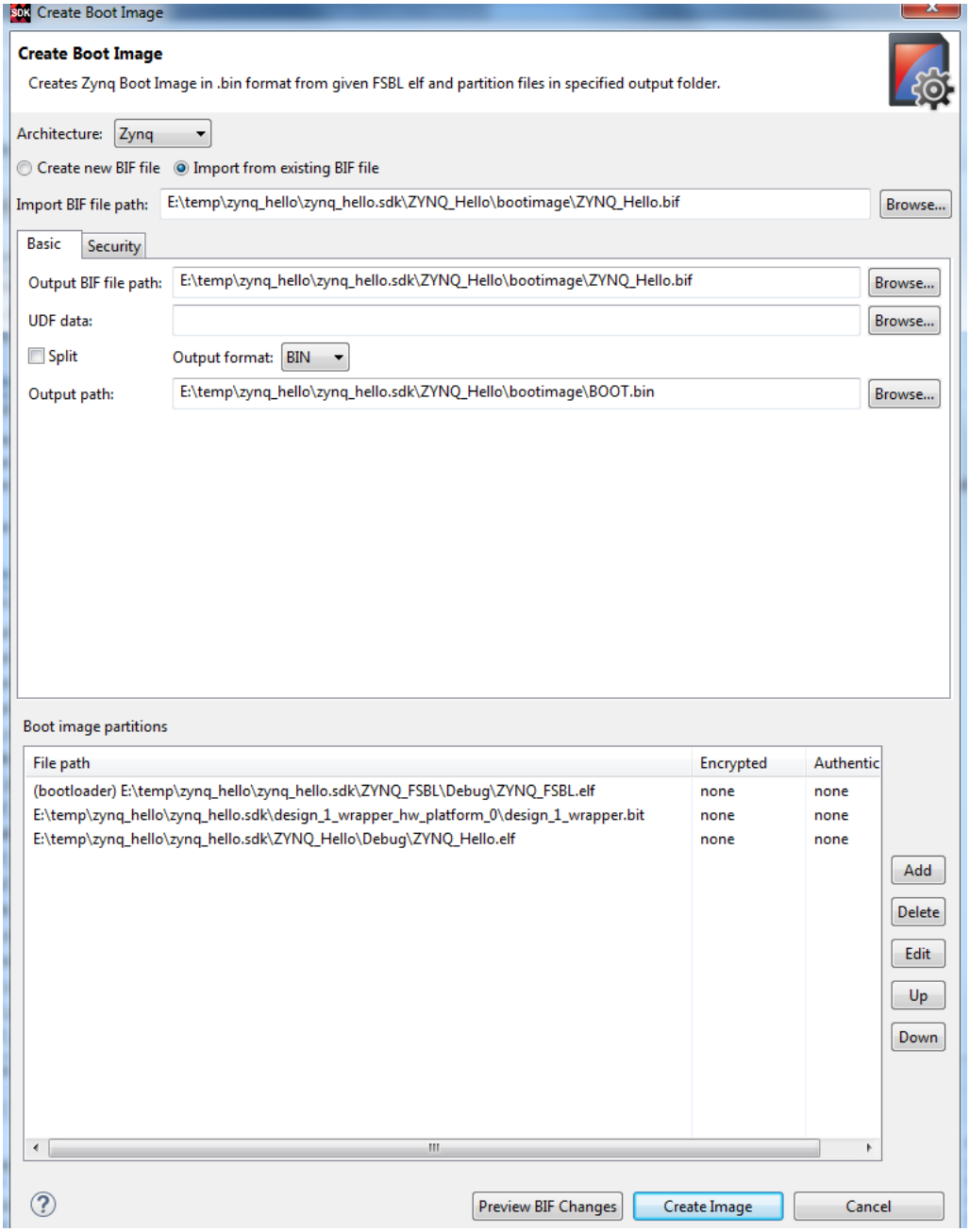



New Project
Templates
Create one of the available templates to generate a fully-functioning application project.
Available Templates:
Dhrystone
Empty Application
Hello World
lwIP Echo Server
Memory Tests
OpenAMP echo-test
OpenAMP matrix multiplication Demo
OpenAMP RPC Demo
Peripheral Tests
RSA Authentication App
Zynq DRAM tests
Zynq FSBL
Let's say 'Hello World' in C.
< Back
Next >
Finish
Cancel

16- Right click ZYNQ_FSBL and set the Flag **-DFSBL_DEBUG_INFO**



17- Right Click on **ZYNQ_Hello** and select **Create Boot Image**



18- **Create Boot Image** and copy **BOOT.BIN** from the following location to **SD Card**

19- Open Tera Term Terminal and configure the correct COM port as shown in Device Manager

20- Press the Reset Button on Z-Turn Board

21- The output is shown below


COM7 - Tera Term VT
File Edit Setup Control Window Help
Xilinx First Stage Boot Loader
Release 2017.3 Feb 13 2018-13:08:01
Devcfg driver initialized
Silicon Version 3.1
Boot mode is SD
SD: rc= 0
SD Init Done
Flash Base Address: 0xE0100000
Reboot status register: 0x60600000
Multiboot Register: 0x0000C000
Image Start Address: 0x00000000
Partition Header Offset:0x00000C80
Partition Count: 3
Partition Number: 1
Header Dump
Image Word Len: 0x000F6EC0
Data Word Len: 0x000F6EC0
Partition Word Len:0x000F6EC0
Load Addr: 0x00000000
Exec Addr: 0x00000000
Partition Start: 0x000065D0
Partition Attr: 0x00000020
Partition Checksum Offset: 0x00000000
Section Count: 0x00000001
Checksum: 0xFFD14B7E
Bitstream
In FsblHookBeforeBitstreamDload function
PCAP:StatusReg = 0x40000A30
PCAP:device ready
PCAP:Clear done
Level Shifter Value = 0xA
Devcfg Status register = 0x40000A30
PCAP:Fabric is Initialized done
PCAP register dump:
PCAP CTRL 0xF8007000: 0x4C00E07F
PCAP LOCK 0xF8007004: 0x0000001A
PCAP CONFIG 0xF8007008: 0x00000508
PCAP ISR 0xF800700C: 0x0802000B
PCAP IMR 0xF8007010: 0xFFFFFFFF
PCAP STATUS 0xF8007014: 0x00002A30
PCAP DMA SRC ADDR 0xF8007018: 0x00100001
PCAP DMA DEST ADDR 0xF800701C: 0xFFFFFFFF
PCAP DMA SRC LEN 0xF8007020: 0x000F6
EC0
PCAP DMA DEST LEN 0xF8007024: 0x000F6EC0
PCAP ROM SHADOW CTRL 0xF8007028: 0xFFFFFFFF
PCAP MBOOT 0xF800702C: 0x0000C000
PCAP SW ID 0xF8007030: 0x00000000
PCAP UNLOCK 0xF8007034: 0x757BDF0D
PCAP MCTRL 0xF8007080: 0x30800100
DMA Done !