

### Zynq UltraScale+ MPSoC (3.2)

Documentation Presets IP Location

#### Page Navigator

Switch To Advanced Mo

PS UltraScale+ Block Design

I/O Configuration

Clock Configuration

DDR Configuration

PS-PL Configuration

#### Clock Configuration

Input Clocks Output Clocks



Search:

Name	Source	Input Freq (MHz)	Range (MHz)
Input Reference frequency			
PSS_REF_CLK	PS_REF_CLK	33.330	27.00 : 60.00
GT Lane Reference frequency			
PCIe	Ref Clk0	100	100
SATA	Ref Clk1	125	125
Display Port	Ref Clk3	27	27
USB0	Ref Clk2	26	26
Peripheral Reference frequency			

OK

Cancel

### Zynq UltraScale+ MPSoc (3.2)

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PS UltraScale+ Block Design

I/O Configuration

Clock Configuration

DDR Configuration

PS-PL Configuration

#### Clock Configuration

Input Clocks Output Clocks

Enable Manual Mode

##### PLL Options

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Search:

Name	Source	FracEn	Requested Freq (MHz)	Divisor 1	Divisor 2	Actual Frequency (MHz)	Range
Low Power Domain Clocks							
Processor/Memory Clocks							
CPU_R5	IOPLL	<input type="checkbox"/>	500	3		499.950043	0.0000...
Peripherals/IO Clocks							
QSPI	IOPLL	<input type="checkbox"/>	125	12	1	124.987511	0.0000...
SDIO1	IOPLL	<input type="checkbox"/>	200	8	1	187.481262	
SD_DLL	IOPLL	<input type="checkbox"/>	1500			1499.850098	
UART0	IOPLL	<input type="checkbox"/>	100	15	1	99.990005	0.0000...
UART1	IOPLL	<input type="checkbox"/>	100	15	1	99.990005	0.0000...
I2C0	IOPLL	<input type="checkbox"/>	100	15	1	99.990005	0.0000...
I2C1	IOPLL	<input type="checkbox"/>	100	15	1	99.990005	0.0000...
CAN1	IOPLL	<input type="checkbox"/>	100	15	1	99.990005	0.0000...
USB0	IOPLL	<input type="checkbox"/>	250	6	1	249.975021	0.0000...
USB3_DUAL	IOPLL	<input type="checkbox"/>	20	25	3	19.998001	0.0000...
Gem3	IOPLL	<input type="checkbox"/>	125	12	1	124.987511	0.0000...
GEM_TSU	IOPLL	<input type="checkbox"/>	250	6	1	249.975021	0.0000...
SWDT0	APB	<input type="checkbox"/>	99.990005			99.990005	0.0000...
TTC0	APB	<input type="checkbox"/>	100.000000			100.000000	0.0000...
TTC1	APB	<input type="checkbox"/>	100.000000			100.000000	0.0000...
TTC2	APB	<input type="checkbox"/>	100.000000			100.000000	0.0000...
TTC3	APB	<input type="checkbox"/>	100.000000			100.000000	0.0000...
CSU_WDT	APB	<input type="checkbox"/>	100.000000			100.000000	0.0000...
PL Fabric Clocks							
<input checked="" type="checkbox"/> PL0	IOPLL	<input type="checkbox"/>	100	15	1	99.990005	0.0000...
<input type="checkbox"/> PL1	RPLL	<input type="checkbox"/>	100	4	1	100	0.0000...
<input type="checkbox"/> PL2	RPLL	<input type="checkbox"/>	100	4	1	100	0.0000...
<input type="checkbox"/> PL3	RPLL	<input type="checkbox"/>	100	4	1	100	0.0000...
System Debug Clocks							
DBG_LPD	IOPLL	<input type="checkbox"/>	250	6		249.975021	0.0000...
Full Power Domain Clocks							
Processor/Memory Clocks							
ACPU	APLL	<input type="checkbox"/>	1200	1		1199.880127	0.0000...
GPU	IOPLL	<input type="checkbox"/>	500	1		499.950043	0.0000...
DDR	DPPLL	<input type="checkbox"/>	533.500	2		533.280029	100.00...
Peripherals/IO Clocks							
DP_VIDEO	VPLL	<input type="checkbox"/>	300	5	1	299.970032	0.0000...
DP_AUDIO	RPLL	<input type="checkbox"/>	25	15	1	24.997501	0.0000...
DP_STC	RPLL	<input type="checkbox"/>	27	14	1	26.783037	0.0000...
PCIE	IOPLL	<input type="checkbox"/>	250	2		249.975021	0.0000...

OK

Cancel

Re-customize IP

## Zynq UltraScale+ MPSoC (3.2)

Documentation Presets IP Location

**Page Navigator**

- Switch To Advanced Mo
- PS UltraScale+ Block Design
- I/O Configuration
- Clock Configuration
- DDR Configuration**
- PS-PL Configuration

### DDR Configuration

Enable DDR Controller

Load DDR Presets: Custom

Clocking Options

Requested Device Frequency (MHz): 1067 Actual Device Frequency: 1066.560059

DDR Controller Options

Memory Type: DDR 4 Effective DRAM Bus Width: 64 Bit

Components: UDIMM ECC: Disabled

DDR Memory Options

Speed Bin (use tooltip): DDR4 2133P	DRAM IC Bus Width (per die): 8 Bits
Cas Latency (cycles): 15	DRAM Device Capacity (per die): 4096 MBits
RAS to CAS Delay (cycles): 15	Bank Group Address Count (Bits): 2
Precharge Time (cycles): 15	Bank Address Count (Bits): 2
Cas Write Latency (cycles): 14	Row Address Count (Bits): 15
tRC (ns): 47.06	Column Address Count (Bits): 10
tRASmin (ns): 33	Dual Rank: <input checked="" type="checkbox"/>
tFAW (ns): 30.0	DDR Size (in Hexa): 0x1FFFFFFF (8GB)
Additive Latency (cycles): 0	

**Other Options**

Memory Address Map: ROW BANK COL	Power Mode Settings
Data Mask and DBI: DM NO DBI	Power Down Enable: <input type="checkbox"/>
Address Mirroring: <input type="checkbox"/>	Clock Stop: <input type="checkbox"/>
2nd Clock: <input type="checkbox"/>	Refresh Mode Settings
Parity: <input type="checkbox"/>	Low-Power Auto Self-Refresh: manual normal
	Temp Controlled Refresh: <input type="checkbox"/>
	Max Operating Temperature: Normal (0-85)
	Fine Granularity Refresh Mode: 1X
	Self Refresh Abort: <input type="checkbox"/>

OK Cancel

Screen clipping taken: 4/16/2019 10:52 AM

