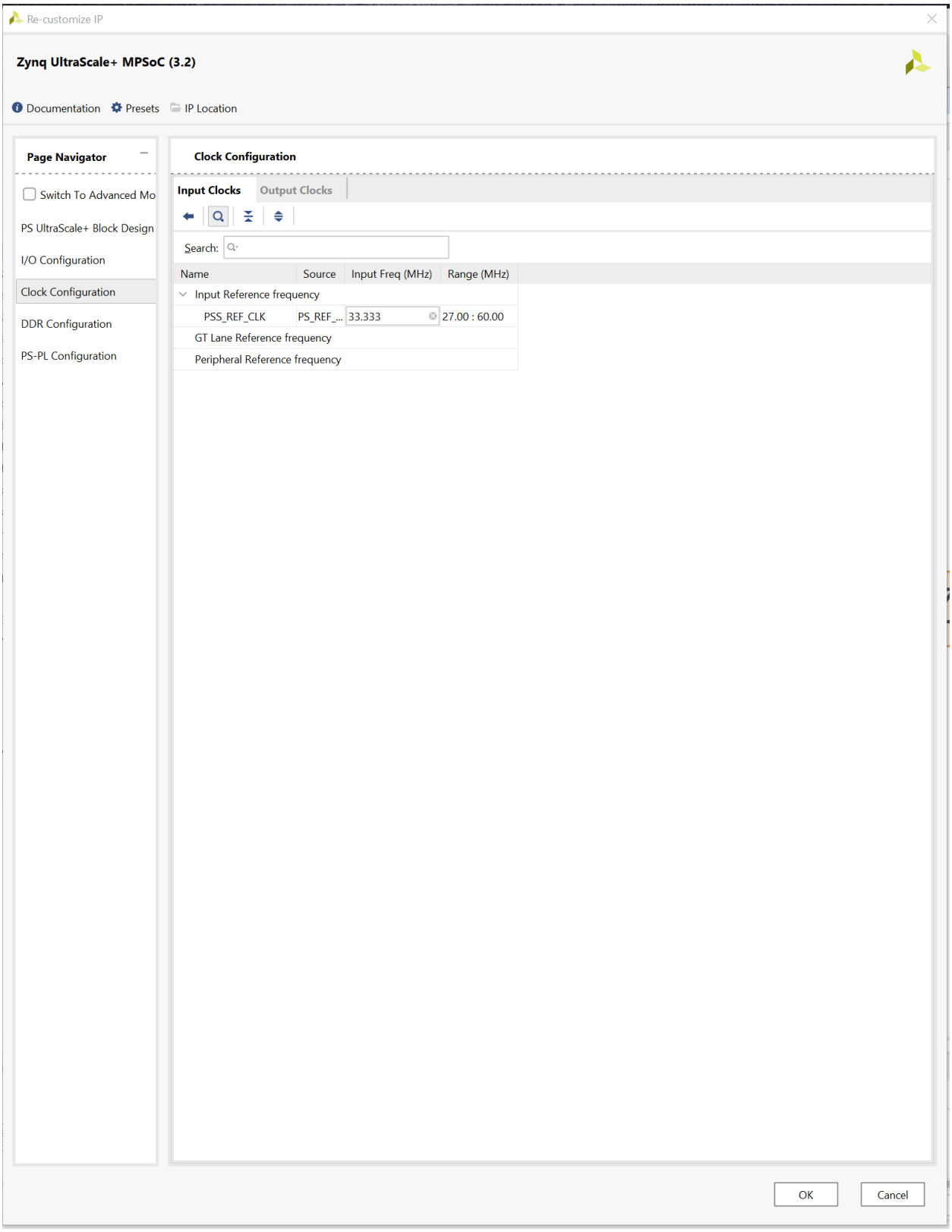
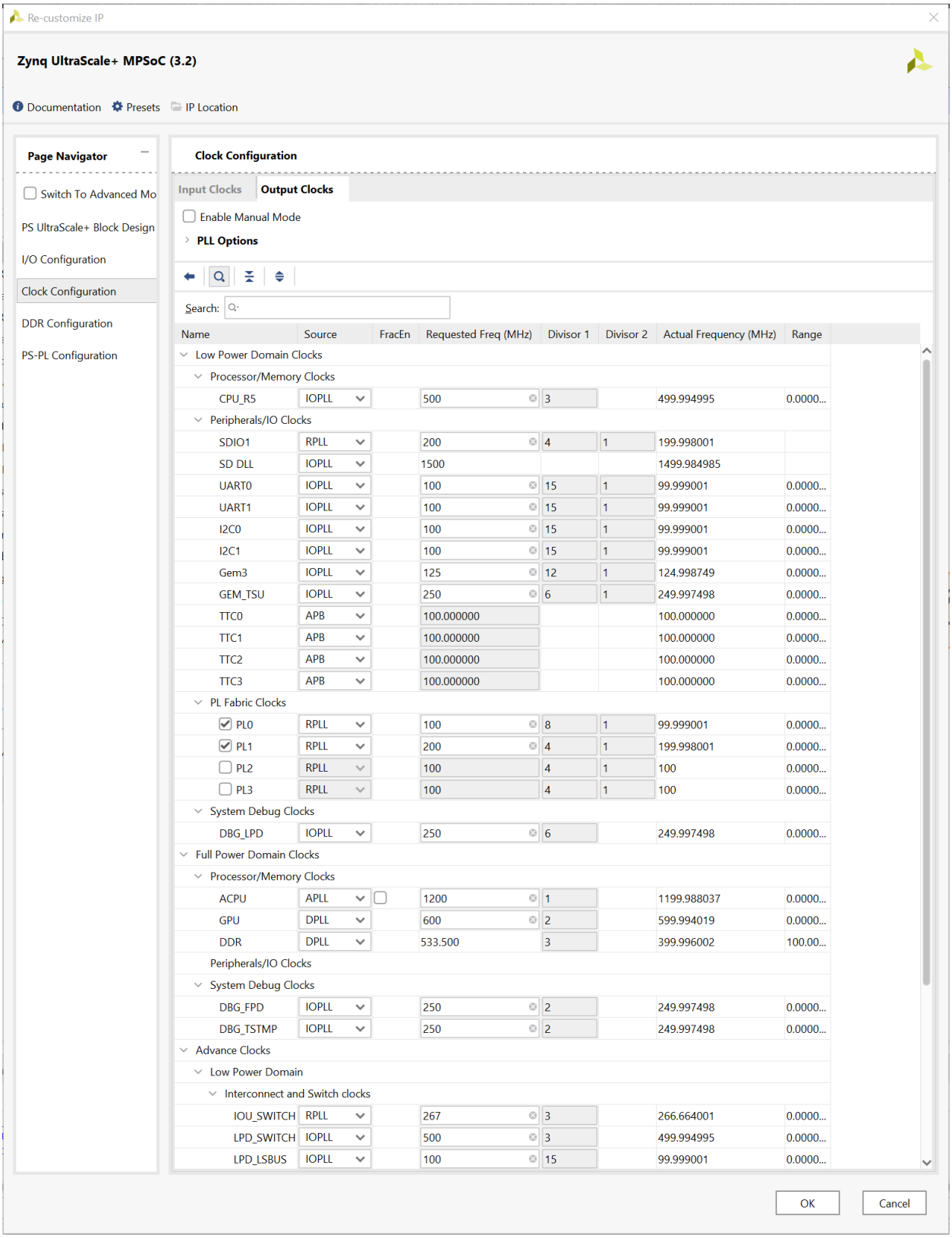
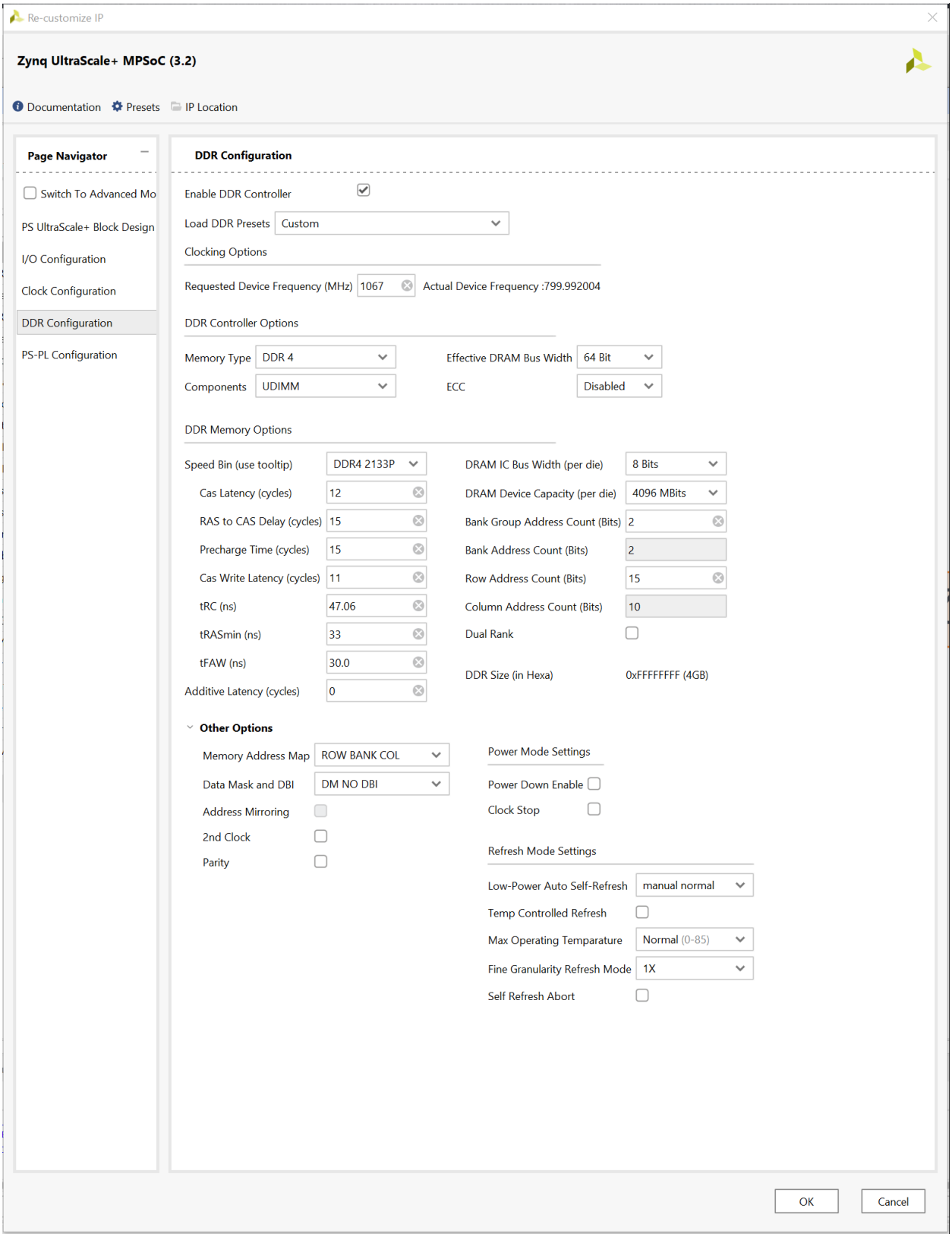


Screen clipping taken: 4/17/2019 11:04 PM


Re-customize IP
Zynq UltraScale+ MPSoC (3.2)
Documentation
Presets
IP Location
Page Navigator
Switch To Advanced Mo
PS UltraScale+ Block Design
I/O Configuration
Clock Configuration
DDR Configuration
PS-PL Configuration
Clock Configuration
Input Clocks
Output Clocks
Enable Manual Mode
PLL Options
Search:
Name
Source
FracEn
Requested Freq (MHz)
Divisor 1
Divisor 2
Actual Frequency (MHz)
Range
Low Power Domain Clocks
Processor/Memory Clocks
CPU_R5 IOPLL 500 3 499.994995 0.0000...
Peripherals/IO Clocks
SDIO1 RPLL 200 4 1 199.998001
SD DLL IOPLL 1500 1499.984985
UART0 IOPLL 100 15 1 99.999001 0.0000...
UART1 IOPLL 100 15 1 99.999001 0.0000...
I2C0 IOPLL 100 15 1 99.999001 0.0000...
I2C1 IOPLL 100 15 1 99.999001 0.0000...
Gem3 IOPLL 125 12 1 124.998749 0.0000...
GEM_TSU IOPLL 250 6 1 249.997498 0.0000...
TTC0 APB 100.000000 100.000000 0.0000...
TTC1 APB 100.000000 100.000000 0.0000...
TTC2 APB 100.000000 100.000000 0.0000...
TTC3 APB 100.000000 100.000000 0.0000...
PL Fabric Clocks
PL0 RPLL 100 8 1 99.999001 0.0000...
PL1 RPLL 200 4 1 199.998001 0.0000...
PL2 RPLL 100 4 1 100 0.0000...
PL3 RPLL 100 4 1 100 0.0000...
System Debug Clocks
DBG_LPD IOPLL 250 6 249.997498 0.0000...
Full Power Domain Clocks
Processor/Memory Clocks
ACPU APLL 1200 1 1199.988037 0.0000...
GPU DPLL 600 2 599.994019 0.0000...
DDR DPLL 533.500 3 399.996002 100.00...
Peripherals/IO Clocks
System Debug Clocks
DBG_FPD IOPLL 250 2 249.997498 0.0000...
DBG_TSTMP IOPLL 250 2 249.997498 0.0000...
Advance Clocks
Low Power Domain
Interconnect and Switch clocks
IOU_SWITCH RPLL 267 3 266.664001 0.0000...
LPD_SWITCH IOPLL 500 3 499.994995 0.0000...
LPD_LSBUS IOPLL 100 15 99.999001 0.0000...
OK
Cancel


Re-customize IP
Zynq UltraScale+ MPSoC (3.2)
Documentation
Presets
IP Location
Page Navigator
Switch To Advanced Mo
PS UltraScale+ Block Design
I/O Configuration
Clock Configuration
DDR Configuration
PS-PL Configuration
DDR Configuration
Enable DDR Controller
Load DDR Presets
Custom
Clocking Options
Requested Device Frequency (MHz)
1067
Actual Device Frequency :799.992004
DDR Controller Options
Memory Type
DDR 4
Effective DRAM Bus Width
64 Bit
Components
UDIMM
ECC
Disabled
DDR Memory Options
Speed Bin (use tooltip)
DDR4 2133P
DRAM IC Bus Width (per die)
8 Bits
Cas Latency (cycles)
12
DRAM Device Capacity (per die)
4096 MBits
RAS to CAS Delay (cycles)
15
Bank Group Address Count (Bits)
2
Precharge Time (cycles)
15
Bank Address Count (Bits)
2
Cas Write Latency (cycles)
11
Row Address Count (Bits)
15
tRC (ns)
47.06
Column Address Count (Bits)
10
tRASmin (ns)
33
Dual Rank
tFAW (ns)
30.0
DDR Size (in Hexa)
0xFFFFFFFF (4GB)
Additive Latency (cycles)
0
Other Options
Memory Address Map
ROW BANK COL
Data Mask and DBI
DM NO DBI
Address Mirroring
2nd Clock
Parity
Power Mode Settings
Power Down Enable
Clock Stop
Refresh Mode Settings
Low-Power Auto Self-Refresh
manual normal
Temp Controlled Refresh
Max Operating Temparature
Normal (0-85)
Fine Granularity Refresh Mode
1X
Self Refresh Abort
OK
Cancel