

```
inout [7:0]                ddr3_dqs_p,
(* mark_debug = "TRUE" *) wire [7:0]  dbg_ddr3_dqs_p,
```

VERSION 1:

```
generate
  if (DEBUG_PORT=="ON") begin: CHIPSCOPE_INST
    /* ... */
    always @(posedge clk) begin
      ddr3_dqs_p_r <= ddr3_dqs_p;
    end

    always @(posedge clk) begin
      ddr3_dqs_p_r1 <= ddr3_dqs_p_r;
    end

    /* ... */
  end
endgenerate
```

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Full Type	Off-Chip Termination	IN_TERM
ddr3_dqs_p_r[15]	INOUT			ddr3_dqs_n	B15	✓	(Multiple)	SSTL15_T_DCI*	1.500	0.750		FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[7]	INOUT			ddr3_dqs_n[7]	F17	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[6]	INOUT			ddr3_dqs_n[6]	F17	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[5]	INOUT			ddr3_dqs_n[5]	G12	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[4]	INOUT			ddr3_dqs_n[4]	L8	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[3]	INOUT			ddr3_dqs_n[3]	A5	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[2]	INOUT			ddr3_dqs_n[2]	E6	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[1]	INOUT			ddr3_dqs_n[1]	J1	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_dqs_p_r[0]	INOUT			ddr3_dqs_n[0]	K3	✓	(Multiple)	DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
ddr3_odt(1)	OUT					✓	(Multiple)	SSTL15*	1.500	0.750		FAST*	NONE	FP_VTT_50	
led(1)	OUT					✓	(Multiple)	(Multiple)*	(Multiple)		12	SLOW	NONE	FP_VTT_50	

Figure 1: ddr3_dqs_p sites are intact (UG954, Table 1-4). Same thing for ddr3_dqs_n.

Basically,

- just followed 'inout' pin (i.e. ddr3_dqs_p) sequentially at memory clock and delayed it by one cycle.
- synthesis and implementation completed successfully (Figure 1).
- but no DQS can be probed since none is attached to any ILA.

VERSION 2:

```
generate
  if (DEBUG_PORT=="ON") begin: CHIPSCOPE_INST
    /* ... */
    IOBUF u_iobuf_ddr3_dqs_p_0
    (
      .I (),
      .T (0),
      .O (ddr3_dqs_p_r[0]),
      .IO (ddr3_dqs_p[0])
    );

    always @(posedge clk) begin
      ddr3_dqs_p_r1 <= ddr3_dqs_p_r;
    end
  end
endgenerate
```

```

assign dbg_dds3_dqs_p = ddr3_dqs_p_r1;
/* ... */
end
endgenerate

```

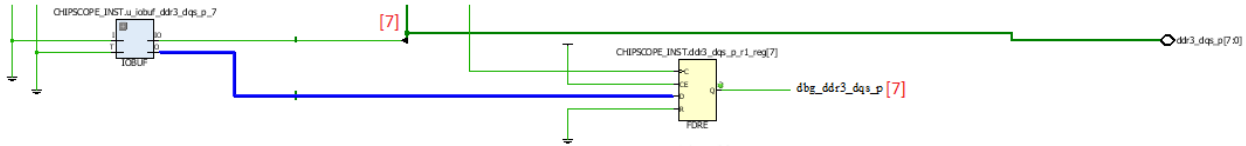


Figure 2: Schematic of Version 2.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Wref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
dds3_dqs_p [5d]	INOUT					[7]	(Multiple)	SSTL15_T_DCI*	1.500	0.750		FAST*	NONE	FP_VTT_50	
dds3_dqs_p [15]	INOUT				dds3_dqs_n			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs_p [7]	INOUT				dds3_dqs_n [7]			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs_p [6]	INOUT				dds3_dqs_n [6]			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs_p [3]	INOUT				dds3_dqs_n [3]			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs_p [4]	INOUT				dds3_dqs_n [4]			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs_p [2]	INOUT				dds3_dqs_n [2]			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs_p [1]	INOUT				dds3_dqs_n [1]			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs_p [0]	INOUT				dds3_dqs_n [0]			DIFF_SSTL15_T_DCI*	1.500			FAST*	NONE	FP_VTT_50	
dds3_dqs [1]	OUT					[7]		34 SSTL15*	1.500	0.750		FAST*	NONE	FP_VTT_50	
led (-)	OUT					[7]		(Multiple) (Multiple)*	(Multiple)		12	SLOW	NONE	FP_VTT_50	

Figure 3: ddr3_dqs_p sites are NOT intact (UG954, Table 1-4).

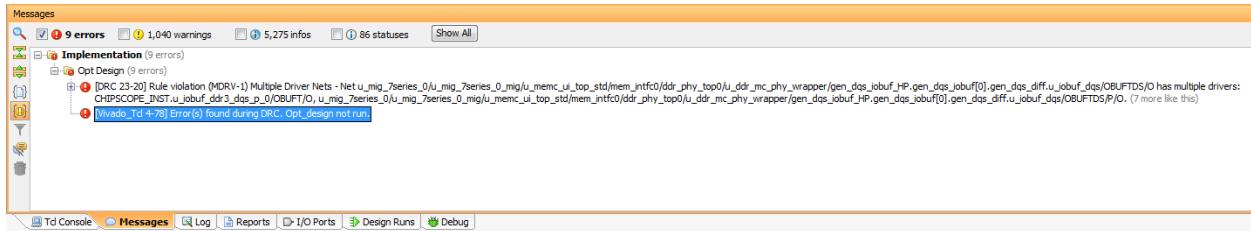


Figure 4: Error Message of Version 2.

Basically,

- just buffered 'inout' pin (i.e. ddr3_dqs_p) and delayed it by one cycle (Figure 2).
- synthesis completed successfully BUT implementation failed (Figures 3 and 4).

Question: Is there anyway I could put 'dbg_dds3_dqs_p' on any ILA in order to probe DQS during normal operation ??