```
inout [7:0]                     ddr3_dqs_p,
(* mark_debug = "TRUE" *) wire [7:0]    dbg_ddr3_dqs_p,
```

VERSION 1:

```
generate
   if (DEBUG_PORT=="ON") begin: CHIPSCOPE_INST
            /* ... */
      always @(posedge clk) begin
        ddr3_dqs_p_r <= ddr3_dqs_p;
      end

      always @(posedge clk) begin
        ddr3_dqs_p_r1 <= ddr3_dqs_p_r;
      end
            /* ... */
   end
endgenerate
```

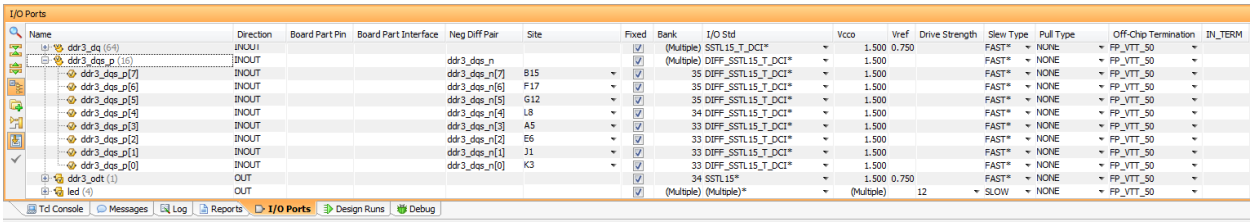

Figure 1: ddr3_dqs_p sites are intact (UG954, Table 1-4). Same thing for ddr3_dqs_n.

Basically,
- just followed ‘inout’ pin (i.e. ddr3_dqs_p) sequentially at memory clock and delayed it by one cycle.
- synthesis and implementation completed successfully (Figure 1).
- but no DQS can be probed since none is attached to any ILA.

VERSION 2:

```
generate
   if (DEBUG_PORT=="ON") begin: CHIPSCOPE_INST
      /* … */
      IOBUF u_iobuf_ddr3_dqs_p_0
      (
        .I   (),
        .T   (0),
        .O  (ddr3_dqs_p_r[0]),
        .IO (ddr3_dqs_p[0])
      );

      always @(posedge clk) begin
        ddr3_dqs_p_r1 <= ddr3_dqs_p_r;
      end
```

```
    assign dbg_ddr3_dqs_p = ddr3_dqs_p_r1;
    /* … */
  end
endgenerate
```

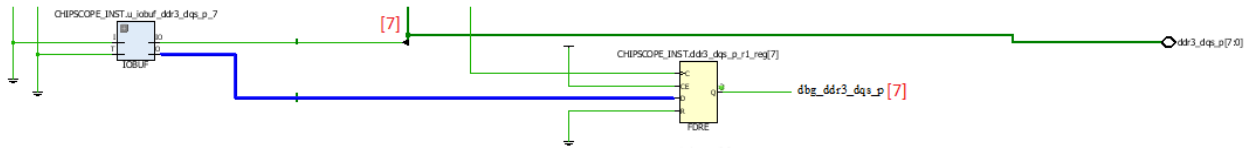

Figure 2: Schematic of Version 2.

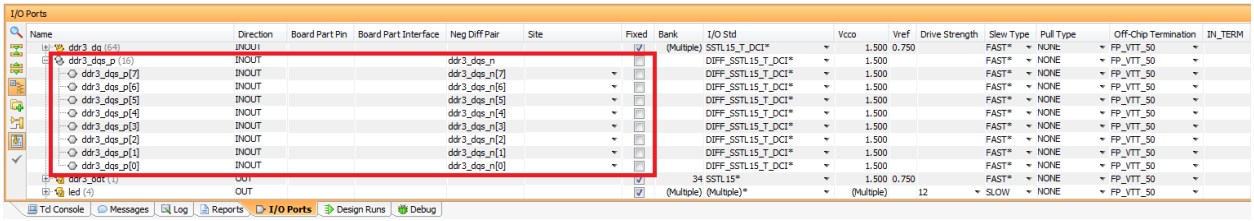

Figure 3: ddr3_dqs_p sites are NOT intact (UG954, Table 1-4).

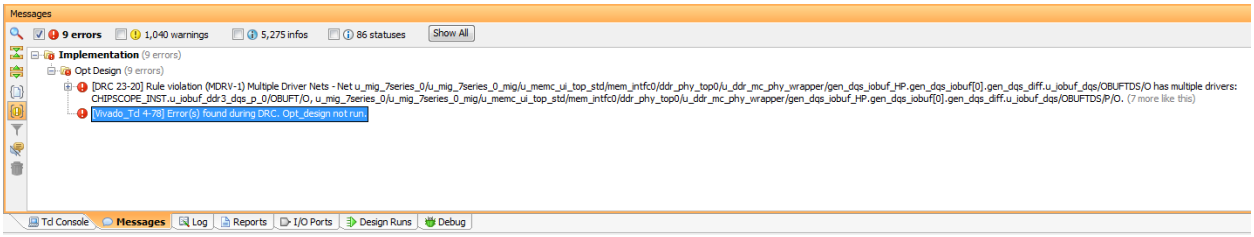

Figure 4: Error Message of Version 2.

Basically,
- just buffered ‘inout’ pin (i.e. ddr3_dqs_p) and delayed it by one cycle (Figure 2).
- synthesis completed successfully BUT implementation failed (Figures 3 and 4).

Question: Is there anyway I could put ‘dbg_ddr3_dqs_p’ on any ILA in order to probe DQS during normal operation ??