--This VHDL code implements a counter of 23 bits. The output of the counter
--provides the signal which selects between the PRBS patterns.

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_unsigned.all;

entity counter is
generic(n: natural :=23);
port( CLK: in std_logic; --The input clock
    count_status : out std_logic :='0' ; --The output signal which selects
    between 2 PRBS patterns.
    rst_L : in std_logic; -- Initial reset of the counter
    counter_value_out : out std_logic_vector(n-1 downto 0); --current value of the
    drp_trigger : out std_logic --the signal that triggers the drp
);
end counter;

architecture Behavioral of counter is
--Defining the internal signals of the design
   signal counter_value: std_logic_vector(n-1 downto 0) := ("000000000000000000000000");
   signal prbs_23_input : std_logic_vector (n-1 downto 0);
   signal counter_status_internal : std_logic ;
   signal trigger : std_logic;
--Defining the PRBS_23 component
component PRBS23
end component;

begin
prbs_23_unit :PRBS23 generic map (23)port map (CLK, prbs_23_input);

process (CLK, rst_L)
begin
if rst_L = '0' then --When the reset value is 0 the counter is loaded with
    initial 0 value.
    counter_value <= "000000000000000000000000";
    counter_status_internal <= '0';
    trigger <= '0';
else
    if (CLK='1' and CLK'event) then
        if (counter_value = ("000000000000000000000000")) then
            trigger <= '1';
            counter_value <= prbs_23_input; --Load a value from the PRBS 23
        to the counter
end if;
end if;
end if;
end process;
counter_status_internal <= not counter_status_internal; -- change the counter status from 0 to 1 and vise versa
  trigger <= '0';
else
  trigger <= '0';
  counter_value <= counter_value - "000000000000000000000001";
-- decrementing the counter value
  counter_status_internal <= counter_status_internal;
end if;
else
  counter_status_internal <= counter_status_internal;
  trigger <= trigger;
end if;
end process;

counter_value_out <= counter_value; -- The actual value of the counter
count_status <= counter_status_internal; -- The status bit acting as the selection signal

-- process (CLK, counter_value
-- begin
-- if (counter_value = "000000000000000000000000" and count_status = '1') then
--
-- trigger <= '1';
--
-- else trigger <= '0';
--
--end if;
--
--end process;
drp_trigger <= trigger;
end Behavioral;