Three Ages of FPGAs

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Some Questions that Might Get Answers Today

- Why are FPGA compile times so long? Are FPGA companies stupid? Or do they just don’t care?
- Why did SRAM FPGAs dominate antifuse FPGAs?
- Why LUTs? Is that a law of nature or what?
- Why did dynamically-programmed FPGAs never go anywhere? Can that change now?
- Why is there no canonical FPGA architecture?
- Whatever happened to reconfigurable computing?
- If the processor is the new LUT, what about processor arrays?
- Whatever happened to multi-chip partitioning for FPGAs?
- What about analog FPGAs? What about asynchronous FPGAs?
- Why don’t FPGA makers offer ASIC conversion?
- Why do FPGA manufactures insist on owning place and route? Will they take over logic synthesis, too? What about high-level synthesis?
- Why should I care about stuff that happened before I was born?
**FPGAs and Moore’s Law**

- **10,000x More Logic**
  - Plus Embedded IP
    - Memory
    - Microprocessor
    - DSP
    - Gigabit Serial I/O
- **100x Faster**
- **5000x Lower Power**
- **10,000x Lower Cost**
The Three Ages of FPGAs

1984-1991 Invention
1992-1999 Expansion
2000-2007 Accumulation
Pre-History: PLD to FPGA

- PLD product terms look like PROM
- Standard PLD models
- PLD delay independent of placement, but scales with inputs and outputs
- PLD logic scales quadratically with inputs
- PLD delay scales linearly with size

- FPGA logic scales with process technology
- FPGA delay independent of inputs and outputs, but dependent on placement
XC2064 The First FPGA (1985)

- 64 flip flops
- 128 3-LUTs
- 58 I/O pins
- 18MHz (toggle)
- 2um 2LM
1985-1991 The Age of Invention

- Tight technology limits
- Efficiency is key
- Must innovate
  - Process: innovation
- No uniformity. Vendors must own tools
- Design automation is secondary to capacity

Applications
- FPGAs are much smaller than the application problem size
- What are they really good for? Emulators? Systolic computation?
- FPGAs are “Glue Logic”
The Architectural Shakeout
The Architectural Shakeout

Mass extinctions in the mid 1990s
Xilinx: 8100, 6200, 4700, Prizm, …
Plessey, Toshiba, Motorola, IBM, ...

We were hit by fast-moving CMOS process technology, particularly multiple metal layers.
Major Environment Change in the 1990s

- LUT Count
- Wire Length

- Ages 10

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ASIC is lower cost than FPGA beyond the crossover point.

The crossover point gets larger every generation.
FPGAs Close on ASICs

Source: Synopsys, Gartner Dataquest, VLSI Technology, Xilinx
The Design Gap

Source: Synopsys, Gartner Dataquest, VLSI Technology, Xilinx
Longer wires give dramatic improvement for “hands-off” design
FPGAs in the Age of Expansion

» Process Technology
  - Rapid scaling with cheap transistors and cheaper interconnect enables large devices
  - Ride the technology wave

» Applications
  - FPGA size approaches the problem size
  - Large reconfigurable devices enable communications and computation applications

» Ease-of-Design Becomes Critical
  - Synthesis flow dominates
  - Interconnect-starved architectures die
50 Million System Gates in 2005!

* assumes 25% of CLBs used as RAM
Virtex-4: A “Platform FPGA”

- 200,000 Flexible Logic Cells
- 500 MHz Digital Clock Management
- 500 MHz, 10Mbits BRAM with FIFO & ECC
- 0.6-11.1 Gbps Serial Transceivers
- AES Design Encryption
- 1 Gbps Source Synchronous I/O
- 450 MHz PowerPC® Processor with Auxiliary Processing Unit
- 500 MHz Programmable DSP Execution Units
- 10/100/1000 Ethernet MAC
Diminishing Return on Scaling

Source: Synopsys, Gartner Dataquest, VLSI Technology, Xilinx
Process Technology

- The end of Dennard scaling: power vs. performance
- Complexity eliminates “casual” ASIC users

Applications

- Bandwidth limits on I/O constrain systems
- FPGAs are larger than the typical problem size
  - Libraries and logic generators
- Users are implementing complete systems
  - Standards: libraries
  - Cost: Low-cost FPGAs
  - Power
2000-2007 The Age of Accumulation

New dimensions in design: heterogeneous system design
The Winning Application: Packet Router

Image: edn.com
2008- The Age of …
Part 1. Technology
Frequency Stagnation

Source: cpubb.stanford.edu
I/O Bandwidth Gap

Source: Xilinx, Inc.

Rent’s Rule

Source: Xilinx, Inc.
Cost Per Transistor Predicted to Rise!

COST PER GATE REDUCTION TRENDS

IBS

WRONG TREND

Cost per Million Gates ($)

90nm: 0.0636
65nm: 0.0521
40nm: 0.0362
28nm: 0.0261
20nm: 0.0275
14nm: 0.0278

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3D: Virtex-7 2000T: I/O Bandwidth and Cost

Low risk approach to integrate TSV & u-bump
- Passive silicon interposer with 65nm interconnects & coarse-pitch TSV

High density micro-bump for 10K-30K chip-to-chip connections

Interposer /Package Technology

<table>
<thead>
<tr>
<th>Technology</th>
<th>Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M4</td>
<td>2um pitch 4X layers</td>
</tr>
<tr>
<td>TSV</td>
<td>12um diameter &amp; 180um pitch</td>
</tr>
<tr>
<td>Micro-bump</td>
<td>45um pitch</td>
</tr>
<tr>
<td>C4</td>
<td>180um pitch</td>
</tr>
<tr>
<td>Package</td>
<td>6-2-6 Layer, 1.0 mm BGA pitch</td>
</tr>
</tbody>
</table>

28nm + 65 nm Interposer

Courtesy of Xilinx, TSMC, Amkor
Heterogeneous 3D Integration: Performance and Power

Enabling breakthrough integration for Nx100G and 400G line-card solutions

Monolithic Device

First 3D FPGA
Based on Stacked Silicon Interconnect

First Heterogeneous 3D FPGA
Based on Stacked Silicon Interconnect

Virtex-7 HT FPGAs

- Deliver leadership bandwidth, power efficiency and signal integrity
- Provide the highest number (16) of 28 Gbps transceivers – 4x the competition
- Enable build-out of economical Nx100G & 400G line cards using CFP2 optical modules
2008- The Age of …
Part 2. Money
Design Cost

Source: Gartner and Xilinx
The Economics of the Design Cost Challenge

Growing ASIC Gaps

- $400M-$800M revenue required to justify 28nm ASICs
- Growing schedule risks, cost and time to change
- Anticipated ASIC supplier gap as vendors struggle to profit

Requires Smarter and ALL Programmable Solutions

Source – IBS, 2013. *Xilinx estimates
2008- The Age of …
Part 3. Applications
Hardware and Software Programmability: ASSP SoC

Estimated FPGA/PLD Design Starts, 2003-2013

Source: Gartner (March 2009), Report: Market Trends - ASIC Design Starts, 2009

- With Microprocessor Core
- Without Microprocessor Core
## One View of Computation in a System

### Design Approach

<table>
<thead>
<tr>
<th></th>
<th>RISC processor</th>
<th>Proc. w/ accels.</th>
<th>Folded datapath</th>
<th>Pipelined datapath</th>
<th>Replicated datapath</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock:sample</td>
<td>1000:1</td>
<td>100:1</td>
<td>10:1</td>
<td>1:1</td>
<td>1:10</td>
</tr>
<tr>
<td>Data Rate (200MHz clock)</td>
<td>200Ks/s</td>
<td>2Ms/s</td>
<td>20Ms/s</td>
<td>200Ms/s</td>
<td>2 Gs/s</td>
</tr>
<tr>
<td>Applications</td>
<td>Human interaction</td>
<td>Communications protocols</td>
<td>Control Low B/W communications</td>
<td>Cryptography Video Signal conditioning</td>
<td>100G packet processing</td>
</tr>
<tr>
<td></td>
<td>Audio</td>
<td>TCP/IP</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ARM A9 processors**: 1-2 Gops

**Fabric**: 10 – 500 Gops

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Zynq All-Programmable SoC

Processor System (PS)
- 2x ARM9 866MHz-1GHz 32K/32K I/D Caches
- 512KB shared L2 Cache
- 256KB On-chip memory
- Memory controller
- Bus interfaces, timers
- Libraries, OSs, middleware

Programmable Logic (PL)
- 28K – 440K LCs
- 240K – 3MB RAM
- 80 – 2020 DSP blocks
- I/O, Transceivers, PCIe, Ethernet…

Programmable ADC
- Inputs from Voltage, Temp sensors

AMBA AXI bus fabric
All-Programmable Programming

Application in C/C++/OpenCL

Platform Information

SW-Centric Design Environment

Kernels using HLS

Binary for CPU

Bitstream for PL fabric

ARM CPUs

Data Movement Interconnect

FPGA Fabric

Zynq device

Memory

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Phenox

- 2 cameras
- Microphone
- 4 motors
- Autonomous
- Avoids obstacles
- Responds to audio signals and hand gestures
- Programmable aerial platform
- Programmed with OpenCL
Phenox

- 2 cameras
- Microphone
- 4 motors
- Autonomous
- Avoids obstacles
What is the next age?
This is the age of the design engineer!
Go build great stuff!