Large Dynamic Range Accurate Digitally Programmable Delay Line with 250-ps Resolution

Jiaqi Li, Zhe Zheng, Min Liu, Siliang Wu
Department of Electronic Engineering, Beijing Institute of Technology, Beijing 100081, P. R. China
E-mail: wjljq@263.net

Abstract

This paper presents a design of large dynamic range accurate digitally programmable delay line with 250-ps resolution on a single field programmable gate array (FPGA) chip. This design adopts Time-to-Digital conversion(TDC) technology, counter-based delay technology and small range digitally programmable delay line technology. When working with an oscillator with frequency accuracy of ±1ppm, and when the delay range is within 0~0.1 ms, the delay accuracy of our design can reach ±350 ps.

1. Introduction

The technology of large dynamic range accurate digitally programmable delay to digital pulse signal is very useful in a great many signal processing systems, especially in the radar echo signal simulating systems.
Conventional digital pulse delay technologies can't resolve the conflict between delay resolution and delay range. For example: (1) Hybrid programmable delay line device， such as AD9501[1], which consists of a linear ramp generator, an digital-to-analog converter (DAC) and a voltage comparator, its resolution is limited by the DAC and the noise performance of the analog parts in the circuit. Furthermore, their delay drift degrades significantly over temperature, especially in case of large delay;(2) Integrated circuit with all-CMOS technology: such as DS1020[2],though it can produce more stable delays than the hybrid programmable delay line, its delay resolution still conflicts with its full scale delay range;(3)Counter-based delay line: digital counter is widely used to generate time delay to a pulse signal. The delay range can be very large, but the delay accuracy is determined by the clock frequency of the counter. This is because the time interval between the rising edge of the input pulse and the rising edge of the counter's clock is randomly changing, in other words, the input pulse and the counter's clock are not phase aligned. For example, if the frequency of the counter's clock is 100MHz, the accuracy of the counter-based delay line is ±5ns,and it is impossible to produce a delay accuracy to the extent of hundreds of ps in this way.

By combining the counter-based delay line with TDC and accurate small range programmable delay line, the conflict between delay resolution and delay range can be solved. First we accurately measure the time interval between the rising edge of the counter's clock and that of the input pulse, then we will be able to compensate for this delay using an accurate small range programmable delay line after the input pulse is delayed by the counter. Thus the final resolution and accuracy is mainly determined by the resolution and accuracy of the TDC and small range programmable delay line..

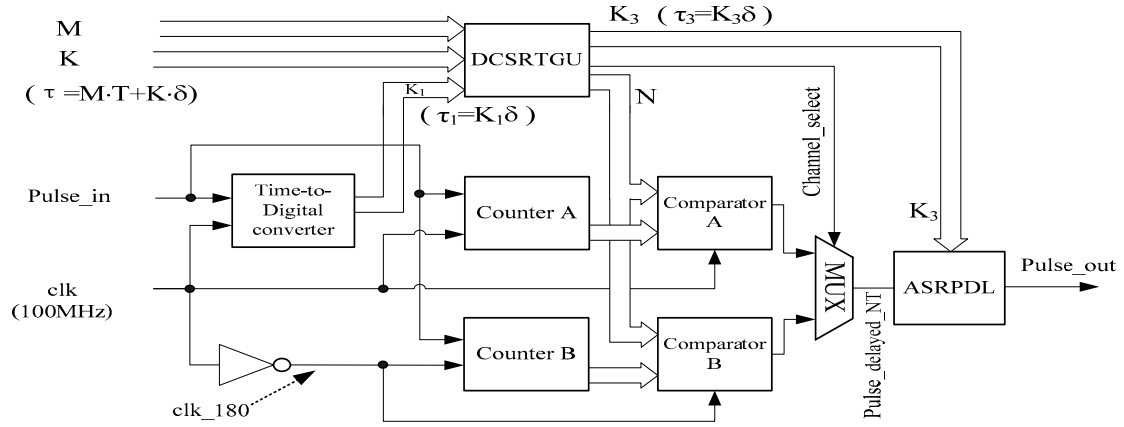

Figure 1. Simplified block diagram of the circuit

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2. The structure and the theory of operation of the circuit

As shown in Figure 1,the delay line circuit consists of the following units: time-to-digital converter(TDC), delay-control signal real time generating unit (DCSRTGU),two counters, two synchronous comparators and accurate small range programmable delay line(ASRPDL).

The circuit shown in Figure 1 has four inputs and one output: ***clk*** is the system clock, ***pulse_in*** is the pulse signal to be delayed, M and K are the two delay control words, ***pulse_out*** is the delayed signal.

The theory of operation of the circuit in Figure 1 is illustrated in Figure 2.

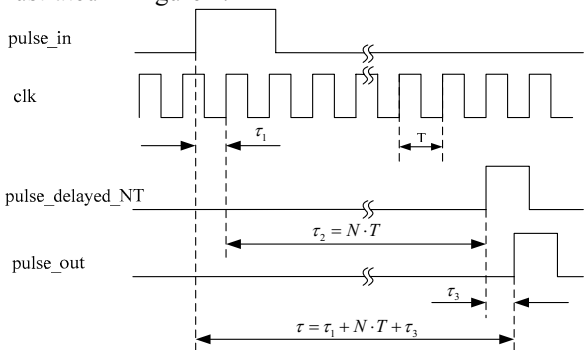

Figure 2. Method for large dynamic range accurate digitally programmable delay line

First, since the time interval(τ_1 ,as shown in Figure 2) between rising edge of the input pulse and the rising edge of the counter's clock is randomly changing, if we can't accurately measure τ_1,it is impossible to accurately delay the input pulse with the counter. The TDC shown in Figure 1 is used to measure τ_1. Secondly, because the time delay(τ) we want to generate to the input pulse may not be equal to the sum of τ_1 and integral number of times of periods of the counter's clock, after being delayed by the counter, the input pulse must then be delayed again with the accurate small range programmable delay line (ASRPDL) unit. The ASRPDL unit is used to generate time delay of τ_3,as shown in Figure 2.So, the original time delay of τ is divided into 3 parts: τ_1,τ_2(τ_2=N·T),τ_3,and τ equals the sum of the three parts of time.

3. The design of TDC

Some conventional high resolution TDC is realized by two tapped delay lines working in a differential mode[3][4][5][6].Though the resolution of this kind of TDC could be very high, it is too complicated to realize in Field-Programmable Gate Array(FPGA). At the time such kind of TDC was invented, the delay time of logic gate is comparatively large, and two tapped delay lines working in a differential mode is the only way to get high resolution. However, nowadays, such kind of design is not necessary due to the development of the semiconductor technology. The delay time of logic gate has become so small that we can realize a high resolution tapped delay line directly by the logic cell of FPGA. For example, The delay value of each MUX element in a FPGA of virtex-II Pro series is between 200 and 300 ps[7].One structure of a new kind of TDC that is easy to realize in FPGA is shown in Figure 3.

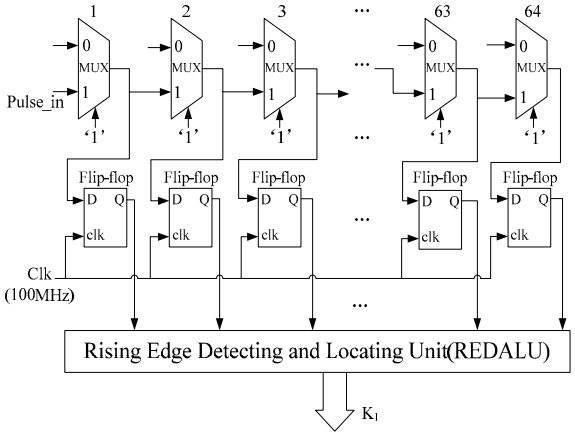

Figure 3. Structure of the TDC circuit

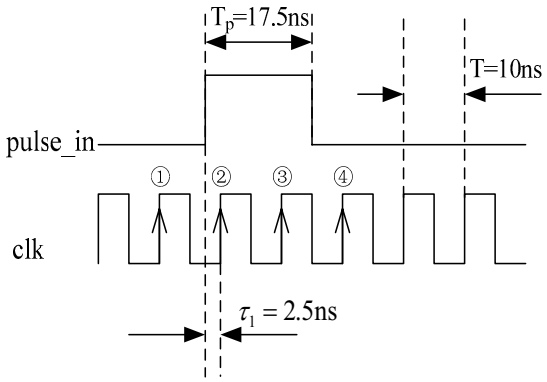

Figure 4. Example of the timing relationship of TDC

As shown in Figure 3, the MUXs are used as delay elements. Before the rising edge of the ***pulse_in*** comes, the output states of all the MUXs are all ZEROs.when the rising edge of the ***pulse_in*** arrives, the states of the MUXs will change into ONEs one by one in turn. When the first rising edge of ***clk*** following the rising edge of ***pulse_in*** comes, the state of all the MUXs will be locked into the D flip-flops. The task of the Rising Edge Detecting and Locating Unit(REDALU) is to determine whether there is a rising edge of ***pulse_in*** in the D flip-flops,and to locate the edge in the D

flip-flops. It should be noted that, because the total delay of the 64-tap delay line is larger than the period of the ***clk***, once a rising edge of ***pulse_in*** goes through the 64-tap delay line ,the edge can be caught by two consecutive rising edges of ***clk***, and only the location of the first time it is caught is used to determine the time interval between the ***pulse_in***'s rising edge and that of the ***clk***'s.For example, as shown in Figure 4,the ***pulse_in***'s rising edge arrives 2.5 ns earlier than the ***clk***'s, the pulse width of ***pulse_in*** is 17.5ns,the delay of each MUX is 250 ps. Under this condition, the states of the 64 MUXs caught by the 4 consecutive rising edges of ***clk*** (labeled in Figure 4)is displayed in Table 1.

Table 1: The states of the 64 MUXs caught by the 4 labeled rising edges of ***clk*** shown in Figure 4

NO.	The values locked into D flip-flops by the 4 labeled rising edges shown in Figure 4	Notes
①	0000000000,0000000000,0000000000,0000000000,0000000000,0000000000,0000	
②	1111111111,0000000000,0000000000,0000000000,0000000000,0000000000,0000	The first time the rising edge of ***pulse_in*** is caught, K_1 is derived from the location of this edge
③	1111111111,1111111111,1111111111,1111111111,1111111111,0000000000,0000	The second time the rising edge of ***pulse_in*** is caught, but this edge is not useful
④	0000000000,0000000000,1111111111,1111111111,1111111111,1111111111,1111	

Under the circumstance in Figure 4, we can easily know that K_1 which is the result of TDC unit equals 10.

4. Delay-control signal real time generating unit(DCSRTGU)

At first, we suppose that the resolution of TDC and accurate small range programmable delay line(ASRPDL) is δ（200ps<δ<300ps）. $\tau=M\cdot T+K\cdot\delta$,M and K are non-negative integers, T is the period of ***clk***, $T\approx K_T\cdot\delta$,$K\cdot\delta<T$. $\tau_1=K_1\cdot\delta+\xi_1$, K_1 is a non-negative integers and it is the result of TDC, ξ_1 is the error of TDC. $\tau_3=K_3\delta+\xi_3$, K_3 is a non-negative integer and it is the output of delay-control signal real time generating unit (DCSRTGU), ξ_3 is the error of ASRPDL.

The task of DCSRTGU is to calculate two numbers: ***N*** and K_3, ***N*** is one of the two inputs of each comparator shown in Figure 1. K_3 is the control code of ASRPDL.

From the basic method introduced previously, we can easily get the formula used to calculate ***N*** and K_3.

$$\begin{cases} N = \mathrm{FLOOR}\left[(\tau-\tau_1)/T\right] \\ K_3 = \mathrm{ROUND}\left[(\tau-\tau_1-NT)/\delta\right] \end{cases} \quad (1)$$

Here, $\mathrm{FLOOR}[\bullet]$ means rounding the element of "$\bullet$" to the nearest integer towards minus infinity, $\mathrm{ROUND}[\bullet]$ means rounding the element of "$\bullet$" to the nearest integer.

Therefore substitute $\tau=M\cdot T+K\cdot\delta$, $\tau_1\approx K_1\cdot\delta$ and $T\approx K_T\cdot\delta$ into Formula (1) we get:

$$\begin{cases} N = \mathrm{FLOOR}\left[(MK_T+K-K_1)/K_T\right] \\ K_3 = MK_T+K-K_1-NK_T \end{cases} \quad (2)$$

In fact, unfortunately, we can't calculate ***N*** and K_3 according Formula (2),that is because: counter A/B(shown in Figure 1) is triggered to begin counting by ***pulse_in***, since the time interval between the rising edge of ***pulse_in*** and the rising edge of the ***clk*** is randomly changing, the rising edge of ***pulse_in*** may fall into the setup/hold window shown in Figure 5,once that happens, metastability will occur, it means that the counter A/B will be triggered earlier or later than the time when we want it to begin counting. For this reason, there must be a unit to adjust the setup time and hold time to avoid the metastability, this unit's detailed function is: when $t_{hold}<\tau_1<T-t_{setup}$, ***clk*** is selected to be the clock of delay counter; when $\tau_1<t_{hold}$ or $\tau_1>T-t_{setup}$, ***clk_180***,which is the inverted signal of ***clk***, is selected to be the clock of delay counter.

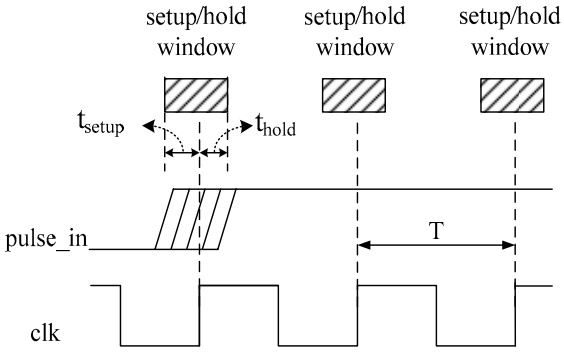

Figure 5. Setup and hold time diagram

In order to have sufficient timing margin, the practical threshold is τ' and τ''. τ' is larger than t_{hold}, and τ'' is smaller than $T-t_{setup}$. Furthermore, τ' and τ'' should meet $\tau''-\tau'>T/2$,this can

guarantee that there is at least one rising edge, either ***clk***'s or ***clk_180***'s ,falling into the shaded areas shown in Figure 6.

According the analysis above, we can get the ***channel_select***'s calculating formula:

$$channel\_select = \begin{cases} 1, & \tau_1' < \tau_1 < \tau_1'' \\ 0, & \tau_1 < \tau' \text{ or } \tau_1 > \tau_1'' \end{cases} \quad (3)$$

channel_select equals ONE means ***clk*** is selected to act as the clock of counter A/B; ***channel_select*** equals ZERO means ***clk_180*** is selected to act as the clock of counter A/B.

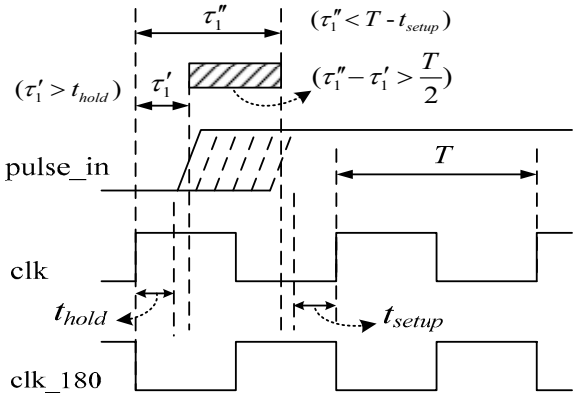

Figure 6. The timing relationship of choice of clock

After resolving the problem of metastability, we know that we can't calculate ***N*** and K_3 simply according to formula (1),because formula (1) does not take into account the phase choice of ***clk***.

The practical formula used to calculate ***N*** and τ_3 is:

$$N = \begin{cases} \text{FLOOR}[(\tau - \tau_1)/T], & \text{when } \tau' < \tau_1 < \tau'' \\ \text{FLOOR}[(\tau - \tau_1 - T/2)/T], & \text{when } \tau_1 < \tau' \\ \text{FLOOR}[(\tau - \tau_1 + T/2)/T], & \text{when } \tau_1 > \tau'' \end{cases} \quad (4)$$

$$\tau_3 = \begin{cases} \tau - \tau_1 - NT, & \text{when } \tau' < \tau_1 < \tau'' \\ \tau - \tau_1 - NT - T/2, & \text{when } \tau_1 < \tau' \\ \tau - \tau_1 - NT + T/2, & \text{when } \tau_1 > \tau'' \end{cases} \quad (5)$$

Substitute $\tau = M \cdot T + K \cdot \delta$, $\tau_1 \approx K_1 \cdot \delta$ and $T \approx K_T \cdot \delta$ into Formula (4) and Formula (5) we get:

$$N = \begin{cases} M + \text{FLOOR}[(K - K_1)/K_T], & \text{when } \tau' < \tau_1 < \tau'' \\ M + \text{FLOOR}[(K - K_1 - K_T/2)/K_T], & \text{when } \tau_1 < \tau' \\ M + \text{FLOOR}[(K - K_1 + K_T/2)/K_T], & \text{when } \tau_1 > \tau'' \end{cases} \quad (6)$$

$$K_3 = \begin{cases} K - K_1 - K_T \cdot \text{FLOOR}[(K - K_1)/K_T], & \text{when } t' < t_1 < t'' \\ K - K_1 - K_T \cdot \text{FLOOR}[(K - K_1 - K_T/2)/K_T] - K_T/2, & \text{when } t_1 < t' \\ K - K_1 - K_T \cdot \text{FLOOR}[(K - K_1 + K_T/2)/K_T] + K_T/2, & \text{when } t_1 > t'' \end{cases} \quad (7)$$

By rearranging Formula (6) and (7),we can get the final calculation formula of ***N*** and K_3,as shown in Table 2.

Table 2: Calculation formula of ***N*** and K_3

Input conditions		Outputs		
Condition 1	Condition 2	Value of N	Value of K_3	Value of channel_select
$\tau'_1 \leqslant \tau_1 \leqslant \tau''_1$	$K - K_1 \geqslant 0$	M	$K - K_1$	1
	$K - K_1 < 0$	M-1	$K - K_1 + K_T$	1
$\tau_1 < \tau'_1$	$K - K_1 - K_T/2 \geqslant 0$	M	$K - K_1 - K_T/2$	0
	$-1 \leqslant K - K_1 - K_T/2 < 0$	M-1	$K - K_1 + K_T/2$	0
	$K - K_1 - K_T/2 < -1$	M-2	$K - K_1 + 3K_T/2$	0
$\tau_1 > \tau''$	$K - K_1 + K_T/2 \geqslant 1$	M+1	$K - K_1 - K_T/2$	0
	$0 \leqslant K - K_1 + K_T/2 < 1$	M	$K - K_1 + K_T/2$	0
	$K - K_1 + K_T/2 < 0$	M-1	$K - K_1 + 3K_T/2$	0

5. Accurate small range programmable delay line(ASRPDL)

Similar to the tapped delay line in TDC unit，the ASRPDL unit is also realized with MUX cells in FPGA, as shown in Figure 7.This unit receives K_3 from DCSRTGU, and then generates the control signal of the 64 MUXs with a 6-64 decoder. The output of the decoder is positive effective.

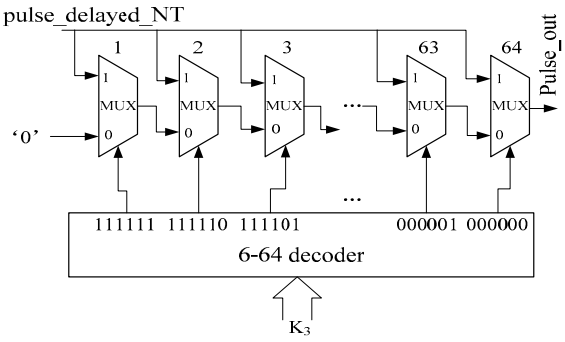

Figure 7. The structure of ASRPDL

6. Calibration and accuracy analysis

Calibration is necessary because the time delay of the delay elements is affected by temperature, power voltage and other factors. Since the drift of accurate small range programmable delay line (ASRPDL) is similar to the tapped delay line of the TDC unit, we can just calibrate the delay line in TDC unit. Because the frequency accuracy of the ***clk*** can be high enough through properly selecting oscillator, the period of ***clk*** can be used as the reference of calibration. If we replace the ***pulse_in*** with ***clk*** in Figure 1,we can know one ***clk***'s period(***T***) equals the total delay of how many taps, in other words, we can get the value of K_T in equation of $T=K_T \cdot \delta$.Then, using the new value of K_T in Table 2 we can get rid of the effect of delay drift.

According the detailed description above, we can know that the main factor that determines the whole circuit's delay accuracy is the tapped delay line's accuracy and the frequency accuracy of ***clk***. Table 3 displays the relationship between delay accuracy and the frequency accuracy of ***clk*** when the resolution of TDC and ASRPDL is 250 ps.

From Table 3 we can see that when the delay range is small, the final delay accuracy is determined mainly by the accuracy of the TDC and ASRPDL; when the delay range is large, the final delay accuracy is determined mainly by the frequency accuracy of ***clk***.

Table 3: Relationship between delay accuracy and the frequency accuracy of ***clk*** (the resolution of TDC and ASRPDL is 250 ps)

Freq. Accuracy of ***clk***	Delay Range	Delay Accuracy
10^{-6}	1us	±251 ps
	1ms	±1250 ps
	1s	±1 us
10^{-8}	1us	±250 ps
	1ms	±260 ps
	1s	±10250 ps

7. Conclusions

A new design of a large dynamic range accurate digitally programmable delay line is introduced in this paper. The design based on this paper can be realized in a single FPGA. This technology will be very useful in radar echo signal simulating systems where range delay is involved. It should be noted that there is still a ***delay hole*** in our design: when $T<\tau<3T$, τ can't be generated in this way, this is because of DCSRTGU's processing time and the delay of synchronous circuits, such as counter and synchronous comparator.

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