FPGA high efficiency, low noise pulse frequency space vector modulation--Part I

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Power modulation is crucial in motor control to ensure high efficiency, fast response time, low ripple torque, low harmonic generation and low acoustic noise. Pulse Width Modulation (PWM) is typically used in continuous methods like Space Vector Modulation (SVM) and discontinuous methods such as Flat-Top Modulation (FTM) exhibit harmonics and require complex mechanisms to mitigate such harmonics. The properties of different modulation methods like Pulse Frequency Modulation (PFM) or Pulse Density Modulation (PDM) can be used advantageously for standalone, or in combination with PWM, to push and spread the noise out of the band of interest, properly shaping the power signal to reduce the acoustic noise, harmonics ripple, distortion, switching losses and the overall modulator complexity.

PFM is clearly beneficial at a modulation index higher than 0.4, thus the realization of a versatile power modulator allowing on-the-fly switching between a space vector PWM and a space vector PFM, coupled with a fast current loop, achieves less switching, a finer torque ripple control and satisfies many motor control applications. This article describes the PWM- PFM versatile modulator, along with its advantages and practical results when applied to Brushless DC (BLDC) motors, Permanent Magnet Synchronous (PMSM) motors and Stepper motors as part of a set of functional motor control libraries implemented for the latest generation of 7 Series All Programmable FPGAs.

Power inverters are at the heart of most power control systems or electrical drives, where digital modulation is used to transfer commanded voltages or currents. Controllable magnitude and frequency are used as a series of high frequency pulses to loads or motors. Power semiconductor switches receive low voltage pulses and transform them into power pulses adequate for the load or motor. The load behaves, in general, as an integrator reconstructing the magnitude and frequency of the original commanded signal.

Real power semiconductor devices, such as MOSFETs, IGBTs, GTOs, etc., experience important limiting factors that decrease the efficient power transfer to the load. This often results in unwanted conduction losses, switching losses, unwanted harmonics, thermal runaway or audible noise. In recent years the overall performance of such power semiconductors has improved, which has opened the door to new design approaches.

Modulation strategy greatly influences the power switch limiting factors. In particular the harmonics produced by the modulation process interacting with electric or magnetic properties of the load produce forces t h a t interfere with mechanical and structural elements creating vibrations and decreasing the load lifetime. Mechanical mitigation strategies to reduce such effects are valid but add extra cost and do not always produce the required result.

Harmonics created by modulation also produce electromagnetic interferences (EMI) that must be minimized to achieve the desired level of electromagnetic compatibility (EMC) required by industry norms and power supply distribution. Mitigation strategies consist o f putting electrical filters and chokes, to block or attenuate such harmonics, but these additional components also result in extra cost and extra space, thus also reducing the reliability of the power systems.

Operating on digital modulation to shape the harmonic contents at the source before being transferred to the load, offers important advantages and avoids or reduces the extra cost required to reduce noise and EMI at the destination.

Power digital modulation has been studied in great detail, but results of such studies are difficult to find. For single-level inverters several pulse-programming methods can be used where the desired voltage waveform may be incorporated into the pulse train by:

- PWM by varying the width of the individual pulses
- PDM by varying the distance between the pulses
- PFM varying the repetition frequency of a pulses train

PWM has found wider applications in power systems as the volt-second balance necessary to recreate intended magnitude at the load can be easily generated. In terms of spectral efficiency, PWM introduces significant harmonics content to the form $6k\pm1\ (k=1\ldots N)$ beyond its fundamental frequency. Such harmonics are directly responsible for the mechanical interactions and EMI issues. PDM and PFM possess better spectral efficiency than PWM providing better EMI mitigation and intrinsic harmonics spreading.

Control

Fast control loops allow management of PDM and PFM at their best. Such modulation techniques have been hindered in high power motors by a combination of power switching limitations and the absence of research. For medium to low power motors the slow speed of the digital current control loop executed by processors or microcontrollers, 100µs…50µs typically, do not have sufficient advantages for the full exploitation of PDM and PFM. Most of the effort to reduce the harmonic content in the modulation signal, without reducing the performance has been focused on elaborate PWM schemes without considering different modulations.

PDM-PFM modulations benefit substantially by having feedback mechanisms that improve their reconstruction fidelity at the load. Feedback requires prompt action by the control system thus a high-speed control loop will make this form of digital-to-analog conversion very advantageous. In modern power systems (see Figure 1), the control is only a part of the c o m p l e t e product; electrical motors and drives require communication supervision, diagnostic and modulators with a great number of timing requirements (see Figure 2) imposing by nature serial and parallel architectures to realize such systems.

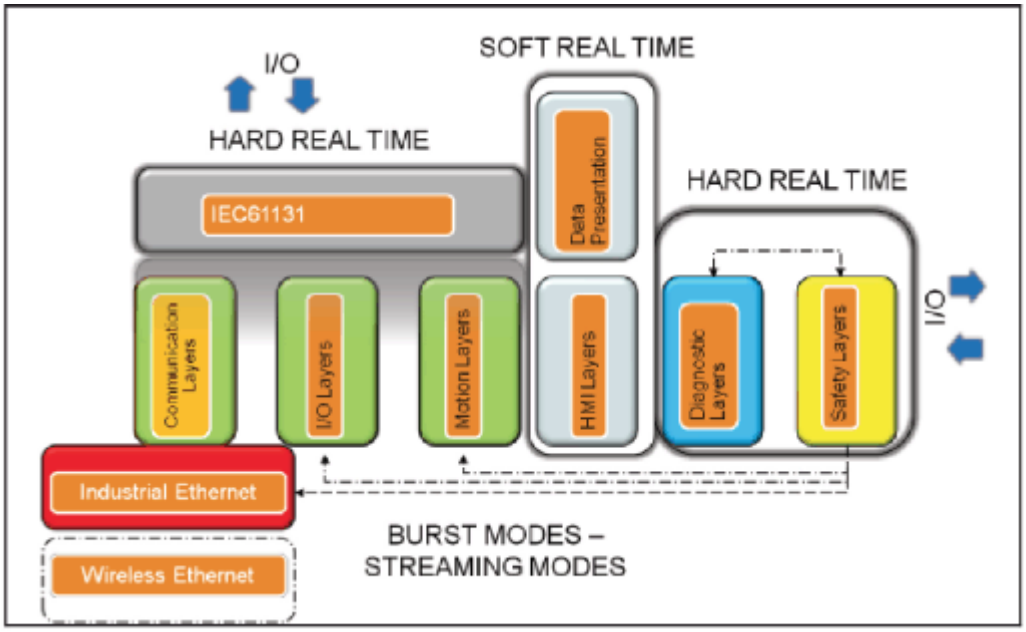

Figure 1. Modern Electrical Drive

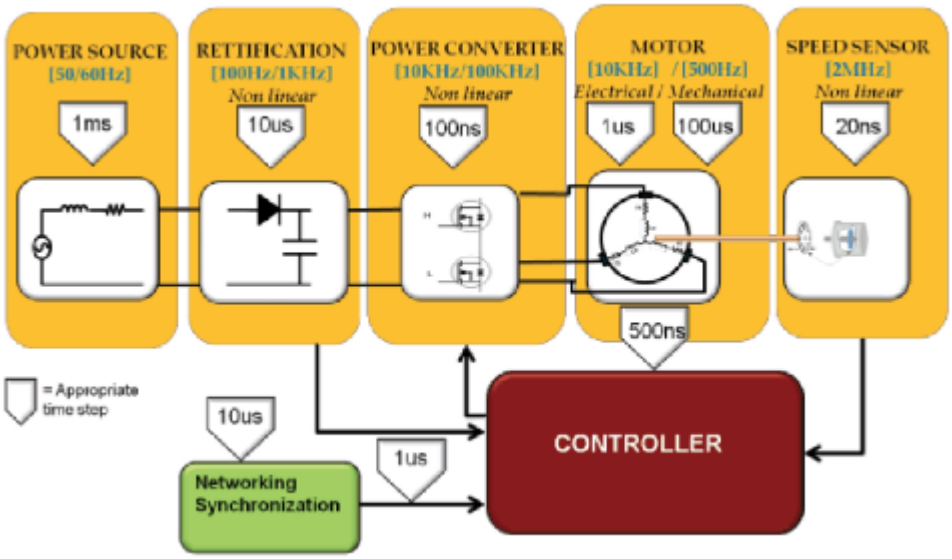

Figure 2. Control Part of Digital Drive

FPGAs are ideal for implementing high-speed control algorithms. The controller realized for a Regenerative Pulse Frequency Modulator (RPFM) is a Field Oriented Control (FOC) implementation, achieving the loop closed in *1µs…2µs*, with moderate *(100MHz…50MHz)* clock frequencies in a low cost FPGA. This is a 50x improvement compared to typical processor driven implementations offering the performance of an analog control.

The RPFM Model

A RPFM is part of a set of libraries for power control systems designed by Xilinx and QDESYS. Sigma Delta Modulation (SDM) is a form of PDM-PFM. RPFM uses SDM to implement the modulator achieving a reduction of EMI via spread spectrum and diminution of acoustic noise. Except for the fundamental there are no prevalent harmonics and less switching losses. The RPFM drives the 3-phase inverter (see Figure 3) via SVM, thus achieving very good linearity, good properties in the over modulation region and automatic dead-time compensation resulting in fine and smooth

transition from the linear modality into the six steps region. Power inverter capabilities are fully exploited and there are many advantages, but there are also some limitations in the lower modulation region. Such limitations have been addressed using a mixed strategy PWM-RPFM resulting in a very versatile and extremely flexible modulator.

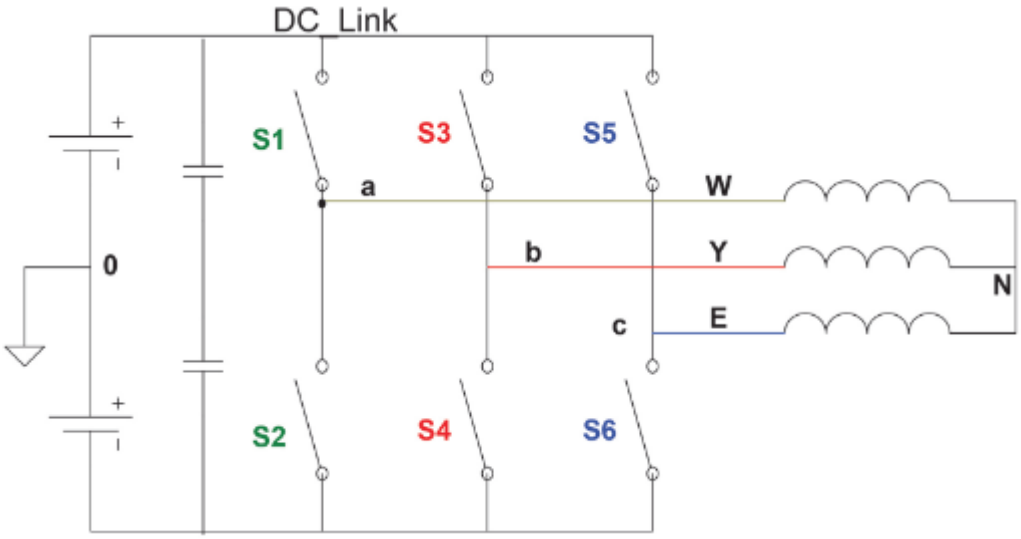

Figure 3. Power Inverter Principle

PWM-RPFM allows a motor's current measurement and control decision at predetermined instants of the RPFM pulse, or every RPFM pulse, a very rapid compensation of the motor's currents trajectories with obvious benefits in the torque ripple and adaption to different motor parameters and operating conditions.

RPFM works by sharing many common elements with the sliding mode control, thus it has been also successfully tested in combination with Sensor-Less Field Oriented Control (SFOC) achieving excellent results especially when combined with Sliding Mode Observers (SMO).

Understanding RPFM

To understand why RPFM is useful consider the process of power modulation as a digital-to- analog conversion (DAC) process. Signal-to-noise properties (SNR) of an N bit DAC follow a digital system as a function of word length and can be expressed by:

$$SNR = 6.02N + 4.77 + 20\ log10(LF)$$

Equation 1

Here N is the number of bits and LF is the loading factor calculated as the ratio between the input signal root mean square (RMS) and the digital-to-analog converter peak voltage.

A three-phase power inverter principle is illustrated in Figure 3 and for each leg it can be considered as a 1-bit DAC having only two possible states: ±DC_Link referenced to the neutral point N and activated by the S1…S6 switches.

Digital control algorithms produce N-bit PCM values that should be transferred to the load. The

inverter delivers only 1-bit thus producing approximately 6 dB SNR as apparent in the Equation 1 setting N=1. SDM can produce the required 6N dB SNR exploiting over-sampling and noise shaping on the 1-bit output achieving the desired output resolution.

FPGA high efficiency--Page 3.
Figure 4 shows a 1-bit SDM DAC composed of a summing point, integrator, switching function, sample and holder (S/H). The S/H output commands the inverter' switches generating the motor voltage *S(t)* that is subtracted from the modulating signal *M(t)* providing the proper scaling.

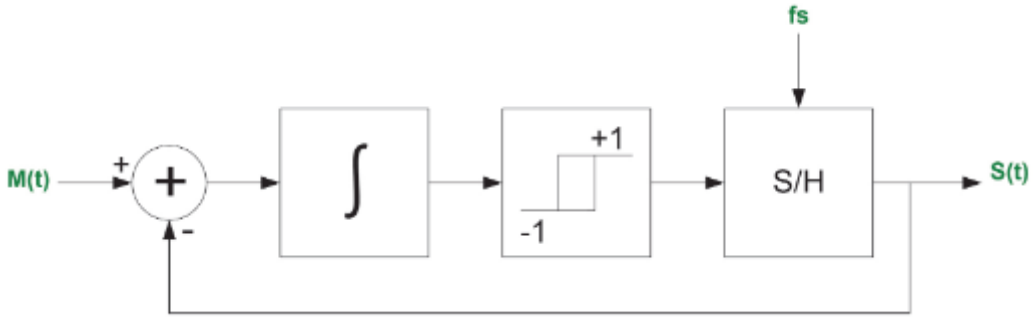

Figure 4. Principle of SDM DAC

M(t) comes from the control algorithm, (FOC or SFOC), the error *e(t) = M(t) – S(t)* is fed into the integrator and its output is applied to a two level switching function generating the ±DC_link via a sample and holder driven at the RPFM pulse frequency *fc*, where the reports of the SNR are in decibels (dBs) for a 1st order SDM as:

$$SNR = 10\log(\sigma_M^2) - 10\log(\sigma_q^2) - \log\left(\frac{\pi^2}{3}\right) + 9.04r$$

Equation 2

Here represent the modulation power and represent the quantizer power, w h e r e *r* is the power of the ratio *fs/fb=2r, fs* is the sampling frequency, and *fb* is the bandwidth of interest. For every doubling of the oversampling ratio, there is an equivalent to incrementing *r,* SNR improves by 9 dB and thus the resolution improves by 1.5 bits.

The pulse trains generated by the modulator need a reconstructing filter to recreate the analog signal. For the case of a motor the reconstructing filter is the motor itself behaving as low pass filter provided the sampling frequency high enough (*fs).*

To analyze RPFM is convenient w h e n transforming the SDM system, shown in Figure 5 and the motor's differential equations into its discrete counterpart. The non-linear quantizer is linearized and modeled by a noise source, *q[n],* added to the signal *M[n],* that produces the quantized output signal *S[n].* The feedback *S[n]* is the modulator's digital sequence ±1 multiplied with the DC_link.

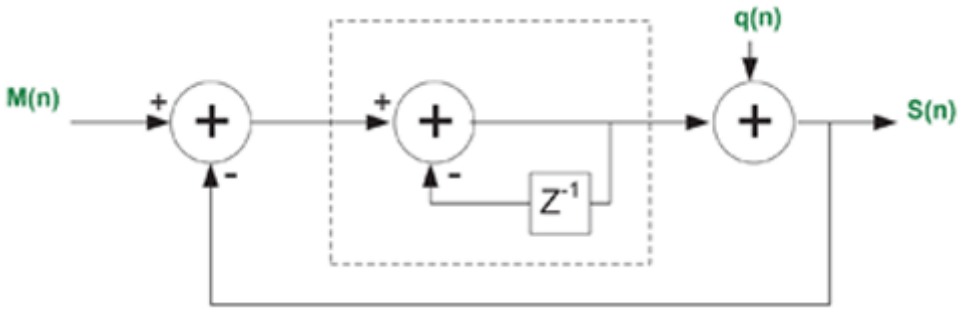

Figure 5. Discrete Version of SDM DAC

RPFM has been tested extensively on three-phase permanent magnet motors, and steppers for the purpose of this article the motor's stator currents in function of stator voltage can be modeled as:

$$is(n+1) = \left(1 - \frac{Rs \cdot dt}{Lm}\right) \cdot is(n) + \frac{dt}{Lm}(Vs - Bemf)$$

Equation 3

Where *Rs* is the primary resistance (phase-phase resistance divided by 2), *Lm* is the primary inductance (phase-phase inductance divided by 2), *is* the stator's current, *Vs* is stator's voltage, Δ*t* is the sampling period (i.e. 1/*fs*) and *Bemf* is the motor back emf; all quantities in bold are in vectorial form. The stator voltage *Vs* is the ±DC_link switching function resulting from the sequence *S[n]*.

Equation 3 represents a first order digital filter, even assuming changes in t he primary resistance and inductance while the motor is operating, the filter form remains the same functioning as the reconstructing filter and in combination the SDM forms a complete first order sigma delta DAC.

The amount of current injected in the motor is directly proportional to train pulses amplitude *Vs*. The feedback *S[n]* in the RPFM modulator is represented by the DC_link, that is the magnitude of *Vs*.

If the DC_link fluctuates it is automatically corrected because of the feedback loop without costly normalizations. The DC_link is transferred integrally at every pulse, thus if it is pulsating, as in the case of a resonant converter, this will make possible the commutation at zero- crossing, with no loss.

Operating bandwidth is a function of the specific motor and RPFM has been tested on very different motors. High-speed motors up to 30000 revolutions per minute (RPM), 1 pair-poles rotating electrical frequencies up to 500Hz and regular motors (between 3600 and 9000 RPM) resulting also in electrical frequencies ranges up to 500Hz due to the higher number of poles. Equation 1 applied to drive such motors shows immediately that with *fs = 1.95us* achieved is a bandwidth *fb* = 500Hz, with a resolution of 11 bits. With *fs = 122ns* the resolution moves to 14bits and *fs = 61ns* resolution moves to 15bits. The noise is also pushed toward higher frequencies, out of the *fb,* as results calculating the transfer function of Figure 5. System partitioning follows an object oriented modular approach because FPGAs are becoming larger and larger in each new generation. The modules can also incorporate an outer control loop that is reassembled to create new functions or complement the already existing one. Monolithic, non modular systems, are very dependent on the

specific implementation, thus are not easily scalable or portable from one product generation to the next and do not allow usage of standalone modules like a RPFM.

$$S(z) = M(z) + (1 - z^{-1})Q(z)$$

Equation 4

To get a better fidelity the reconstruction filter should behave as a higher order filter. Line filters are normally present to reduce EMI. However, and this is the most important point, the RPFM is in the loop of a high speed FOC that closes its loop at *fs* period, correcting the residual error. This is achieved via the modulation command *M[n]* in function of the feedback current reducing the residual in-band noise behaving as higher order filter.

Next: MODULAR FOC

About the Author

Dr. Giulio Corradi *a Senior System Architect with the Xilinx Industrial, Scientific and Medical (ISM) group in Munich, Germany. He has 25 year of experience in management, software engineering and development of ASICs and FPGA in industrial, automation and medical systems, specifically in the field of control and communication for major corporations. DSP algorithms, applied chromatography, motor control, real-time communication, and functional safety have been his major focus. In the years 1997 – 2005 he managed several European funded research projects for train communication networking and wireless remote diagnostic systems. From 2000-2005, he headed the IEC61375 conformance test standard. In 2006, Dr. Corradi joined the Xilinx Munich office contributing to the Industrial Networking and Motor Control reference platforms, providing customer guidance on functional safety applications.*

Dr. Corradi holds a Doctorate degree in Electronic Engineering from the University of Padua (Italy) he also has a long standing collaboration as co-advisor, on DSP, control systems and microelectronic systems. He is active with the Karlsruhe Institute of Technology (Germany) for safety systems, University of Cergy-Pointoise (France) and University of Maribor (Slovenia) for power systems.