FPGA high efficiency, low noise pulse frequency vector modulation—Part II

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Part I

MODULAR FOC

From a practical standpoint the RPFM is an integral part of the high performance FOC built around 15 full-parameterized VHDL library modules for power systems controllers. All the modules are partitioned in functional blocks that can be used stand alone or grouped to achieve higher-level functions. Modules are tuned for performance, minimum footprint and very high resolution using a DSP48 is a multiplier accumulator unit (MAC) used as a building block.

The DSP48 offers 48-bit precision, every library module is implemented around one DSP48 and a single FPGA containing many DSP48. Figure 6 shows the FOC, every block in the diagram is a module library component implementing the current control. Communication between different components happens in form of a start/ready paradigm, thus it is possible to create chains of modules cascading them.

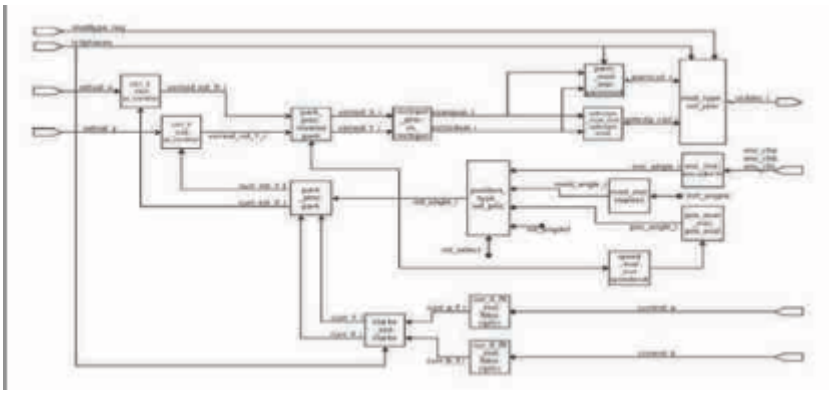

Figure 6. Modular FOC

The FOC is a container for the other specialized IPs functions: encoder signal interface, low pass filter (first order), Clarke transformation, p ark and inverse park transformation, proportional

integral (PI) control, Cartesian to polar transformation, PWM, RPFM, currents synchronization and logging (not shown in Figure 6).

Start event	End of execution	Clock Cycles	Time @ 50 MHz	Time @ 100 MHz
Curr_sync	Pwm(2-phases)	195	3.90 µS	1.95 µS
Curr_sync	Pwm(3-phases)	208	4.16 µS	2.08 µS
Curr_sync	RPFM(3-phases)	179	3.58 µS	1.79 µS

Figure 7. FOC Execution Times

PWM MODULATOR

The PWM modulator is based on the zero-sequence-injection and belongs to carrier- based PWM methods. It allows continuous and discontinuous modulation.

In continuous modulation the waveforms are always creating conditions for an on and off switching of the inverter legs. In the discontinuous modulation the waveforms phase has at least one segment clamped to the positive or negative DC_link for an angle not exceeding 120°, as a consequence the corresponding inverter leg discontinues the modulation.

Continuous and discontinuous modulations have different waveform quality and different linearity characteristics. Most notably the ceasing of modulation creates no switching losses.

For the implementation of this IP in an FPGA, the triangle intersection method has been chosen. One might wonder why the old triangle intersection method and not the direct digital implementation are used. The fundamental reason is a simpler FPGA implementation, reducing the foot print due to elimination of many calculations, switching on the fly between continuous and discontinuous mode, and compensation of DC link embedded in the algorithm.

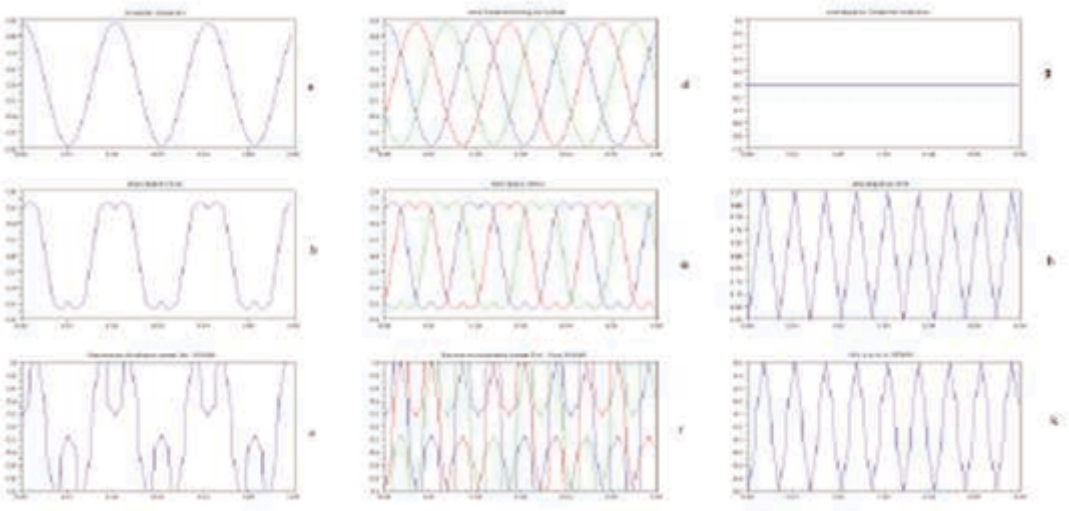

Figure 8. Sinusoidal, Space Vector and Discontinuous PWM3 columns (a),(b),(c), zero-sequence (g),(h),(k), 3-phase result (d),(e),(f).

Figure 8 shows the first three of nine modulation schemes allowed by the implementation and such waveforms comes from:

1. 256 points interpolated look-up table to generate the 3-phase signals @ 18bits precision;

2. On-the-fly selector of four modulation methods: Sinusoidal PWM and SVM-PWM as default, and the other two are selected by the user;

3. Selector between scalar and vector input

- modulation index and angle of the rotating vector - scalar;
- d-q vectors - vectorial;

4. Easily extended in precision, modulated and modified by the user to include additional or different waves

The linear region (yellow and red shown in Figure 9) is handled by the PWM-RPFM and the non linear region (blue is much simply handled only by the RPFM). Switching on the fly between PWM at a lower modulation index and to the RPFM when the modulation index is beyond 0.4 proves very advantageous.

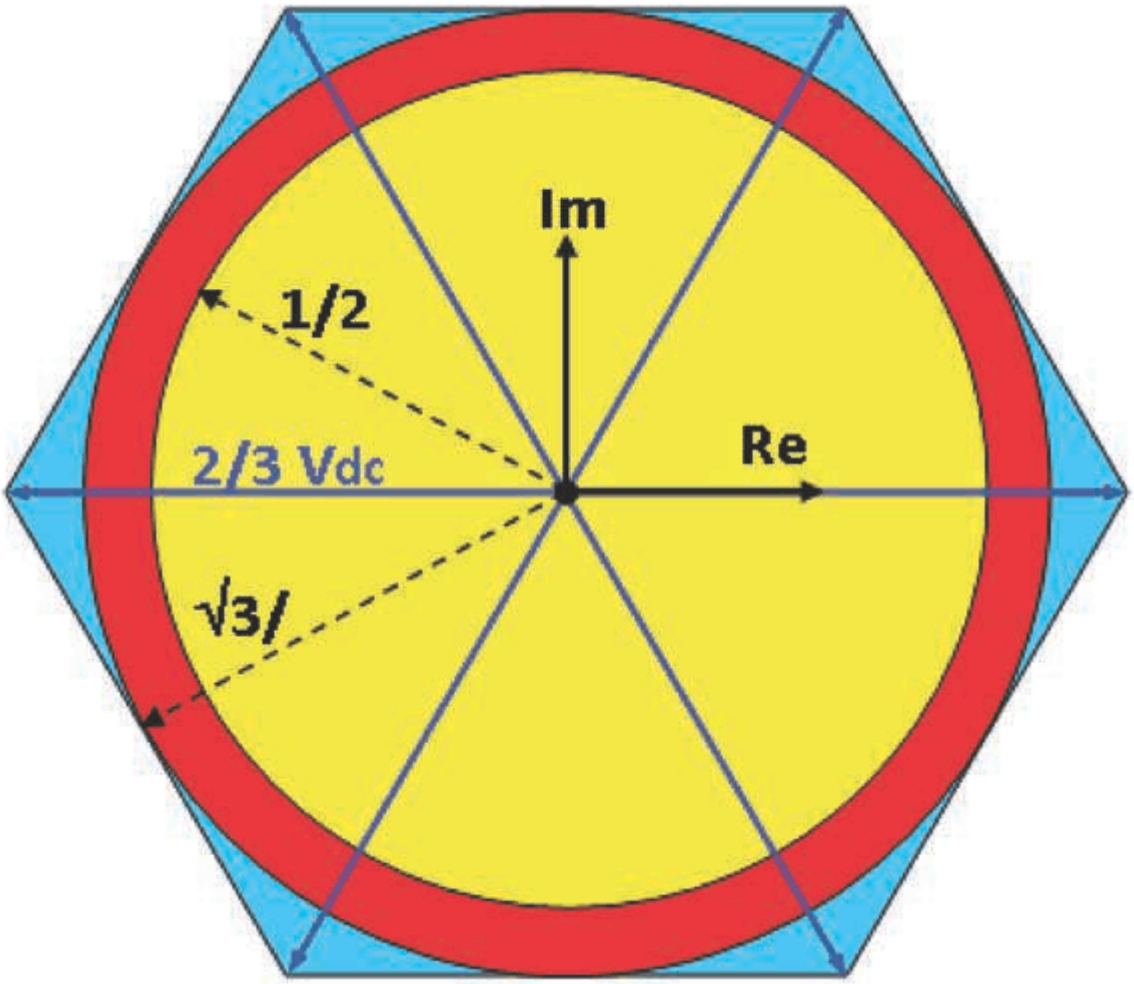

Figure 9. Switching state vectors in the complex plane

Conclusion

The FFT of RPFM shown in Figure 10 shows the spectral distribution very clearly with no dominant harmonics beyond the fundamental. While the PWM in Figure 11 generates significant harmonics, the reconstructed signal is shown in Figure 12; the switches are clearly visible and active only two out of three, with significant reduction of the switches losses. Figure 13 shows the space-vector trajectories in which the current ripple is low; the example shows a frequency of 170 Hz and a RPFM pulse @10µs. This is a very condensed view of the many possibilities and performances of the proposed system.

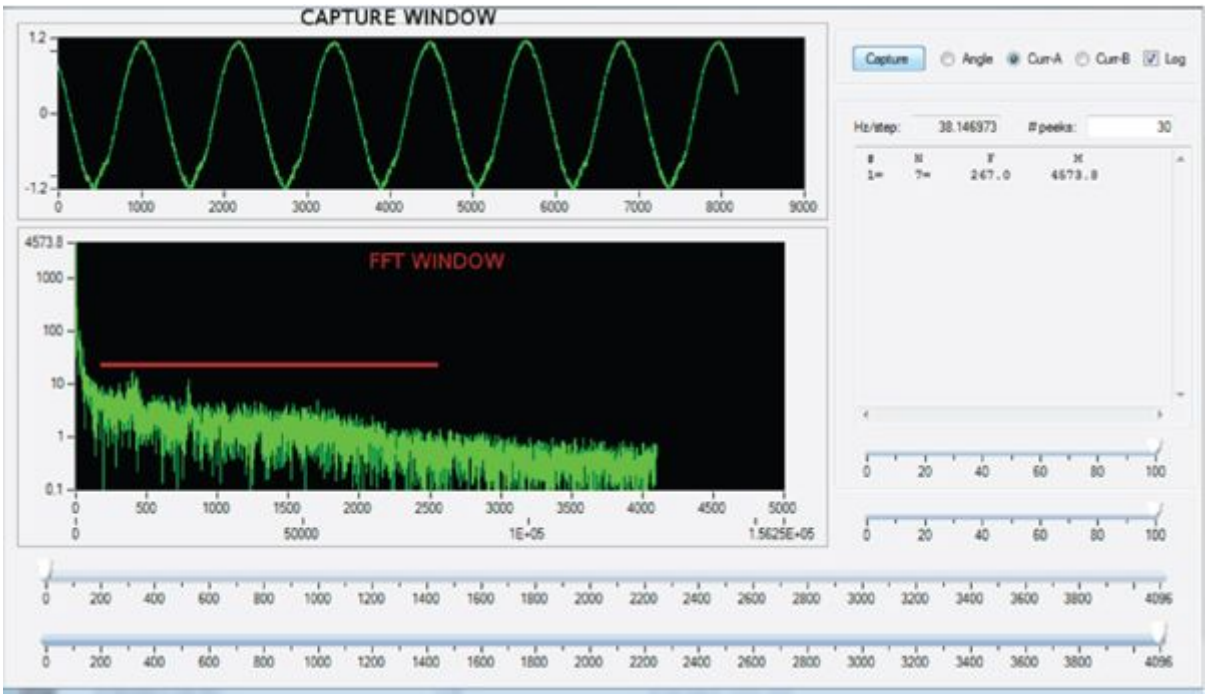

Figure 10. RPFM – Fast Fourier Transform

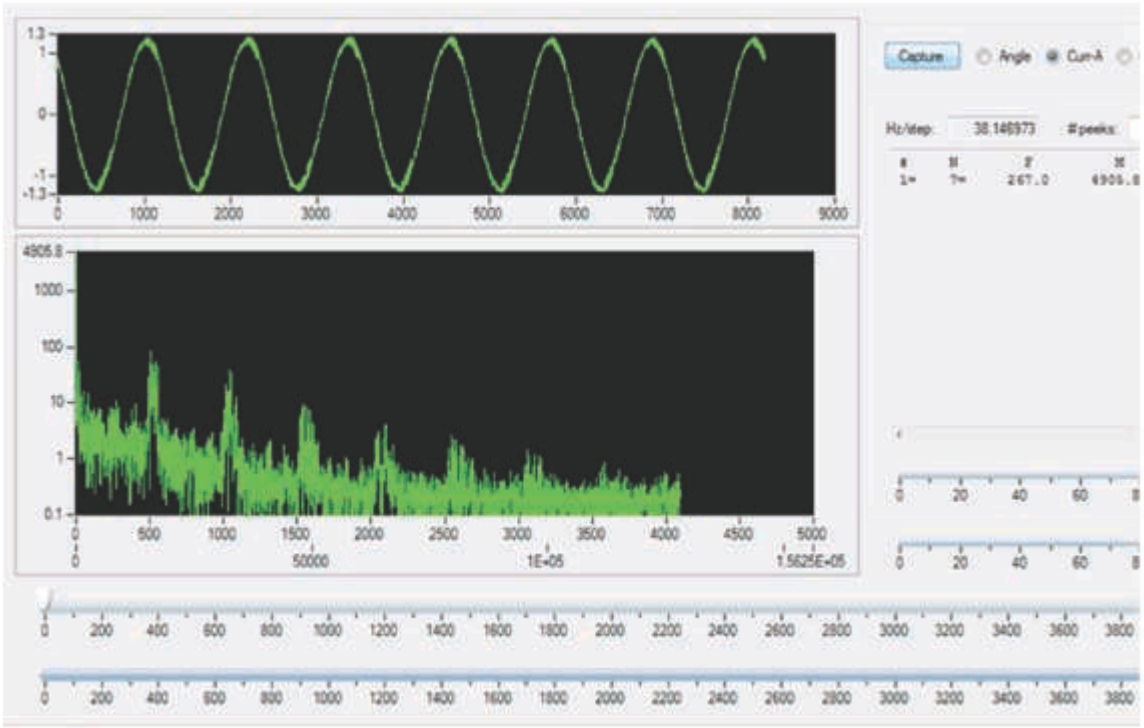

Figure 11. PWM – Fast Fourier Transform

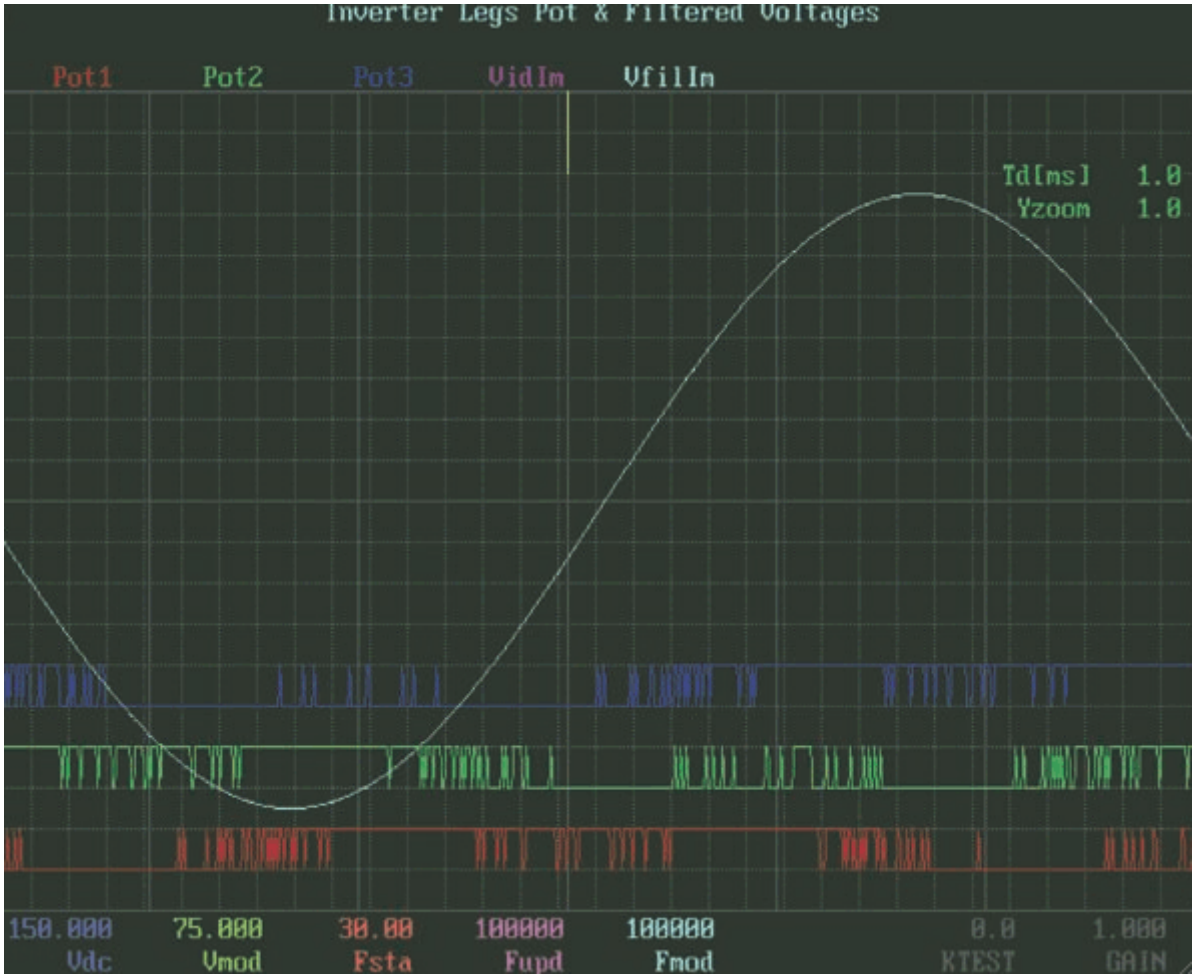

Figure 12. RPFM – Waveform at the load (cyan) and pulses on the inverter Phase E (blue), Phase Y (green), Phase W (red) – Note: only two legs out of three are active at any given time.

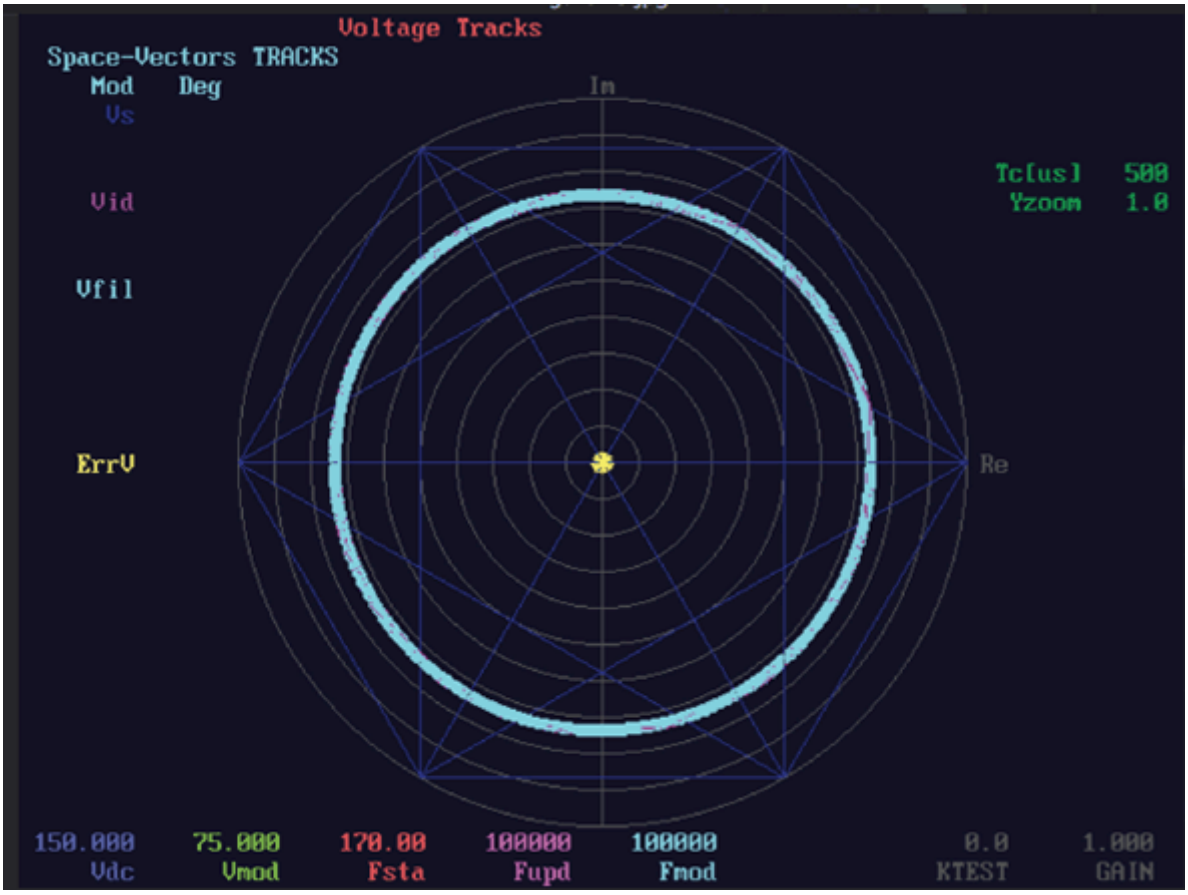

Figure 13. Space-Vectors track – Trajectories (cyan), error (yellow)

About the Authors

Dr. Giulio Corradi a Senior System Architect with the Xilinx Industrial, Scientific and Medical (ISM) group in Munich, Germany. He brings 25 year of experience of management, software engineering and development of ASICs and FPGA in industrial, automation and medical systems specifically in the field of control and communication for the major corporations. DSP algorithms, applied chromatography, motor control, real-time communication, and functional safety have been his major focus. In the years 1997 – 2005 he managed several European funded research projects for train communication networking and wireless remote diagnostic systems. From 2000-2005, he headed the IEC61375 conformance test standard. In 2006, Dr. Corradi joined the Xilinx Munich office contributing to the Industrial Networking and Motor Control reference platforms, providing customer guidance on functional safety applications.

Dr. Corradi holds a Doctorate degree in Electronic Engineering from the University of Padua (Italy) he also has a long standing collaboration as co-advisor, on DSP, control systems and microelectronic systems. He is active with the Karlsruhe Institute of Technology (Germany) for safety systems, University of Cergy-Pointoise (France) and University of Maribor (Slovenia) for power systems.

Diego Quagreda has more than 25 years of professional experience in software for embedded systems, FPGAs and programmable systems. Since 2006 he has been the principal of QDESYS, a company specializing in software for communication, control and embedded systems. Previously he

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Professor Dr. Roberto Raffaetà has more than 40 years of professional experience in designing industrial, scientific, medical and transportation systems as a consultant for major corporations. Roberto specializes in advanced algorithms for motor control, motion control, thermoregulatory systems for gas chromatography and communication systems. He is also a prolific inventor and holds several patents. He holds a Dr. of Ing. degree in Electrical Engineer from the Polytechnic of Milano and has been active as full time professor, involved in research activities with several universities and has actively collaborated in European research projects including the IEC 61375 international standard.